COMPAL CONFIDENTIAL

MODEL NAME : ZAM60

Board NO : LA-A891P

GPIO MAP : 3.6C

PCB NO : DAA0007X000

BOM P/N :

4519R631L06	CPU HSW i3 SR1EN D0 1.9G	SA00007TA0L
4519R631L16	CPU HSW i3 SR1EN D0 1.9G	SA00007TA0L
4519R631L08	CPU HSW i5 SR1EE D0 2G	SA00007MU2L
4519R631L09	CPU HSW i5 SR1EE D0 2G	SA00007MU2L
4519R631L18	CPU HSW i5 SR1EE D0 2G	SA00007MU2L
4519R631L07	CPU HSW i5 Trans SR1EF D0 1.7G	SA00007LO2L
4519R631L17	CPU HSW i5 Trans SR1EF D0 1.7G	SA00007LO2L
4519R631L20	CPU HSW Celeron SR1DX D0 1.6G	SA00007G11L
4519R631L22	CPU BDW i3 QH18 E0 2G	SA000083D0L
4519R631L23	CPU BDW i3 QH18 E0 2G	SA000083D0L
4519R631L26	CPU BDW i5 QH16 E0 2G	SA000083B0L
4519R631L27	CPU BDW i5 QH16 E0 2G	SA000083B0L
4519R631L24	CPU BDW i5 Trans QH17 E0 2G	SA000083C0L
4519R631L25	CPU BDW i5 Trans QH17 E0 2G	SA000083C0L
4519R631L10	CPU BDW i7 QH14 E0 2.2G	SA00008390L
4519R631L11	CPU BDW i7 QH14 E0 2.2G	SA00008390L
4519R631L21	CPU BDW Celeron QGZ5 E0 1.7G	SA000083G0L

SATA Re-Driver (UN2)	Source	X76 P/N	Page
PERICOM (SA00004H100)	main source	X7659631L04	20
TI (SA00003ZX00)	2nd source	X7659631L05	
PARADE (SA00007JU00)	3rd source	X7659631L06	

ROM part	Source	X76 P/N	Page
UC2 (SA000039A30) UC3 (SA00003K820)	main (WINBOND)	X7659631L01	7
UC2 (SA00005L100) UC3 (SA00005KR00)	2nd (MICRON)	X7659631L02	
UC2 (SA00006MK00) UC3 (SA00006AR00)	3rd (EON)	X7659631L03	

MB PCB

Part Number	Description
DAA0007X000	PCB 13O LA-A891P REV0 MB UMA WITH DOCK 1

Layout Dell logo

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REV: A00
PWB: 84J8X
DATE: 1429-04

Power CKT: 0710

Houston 12" UMA Dock M/B

Broadwell U Processor

2014-08-04

REV : 1.0 (A00)

@ : Nopop Component
EMC@ : EMI, ESD and RF Component
@EMC@ : EMI, ESD and RF Nopop Component
XDP@ : XDP Component
CONN@ : Connector Component
VPRO@ : VPRO Component
HSW@ : HSW Component
BDW@ : BDW Component
X76@ : X76 Component

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Title: Cover Sheet

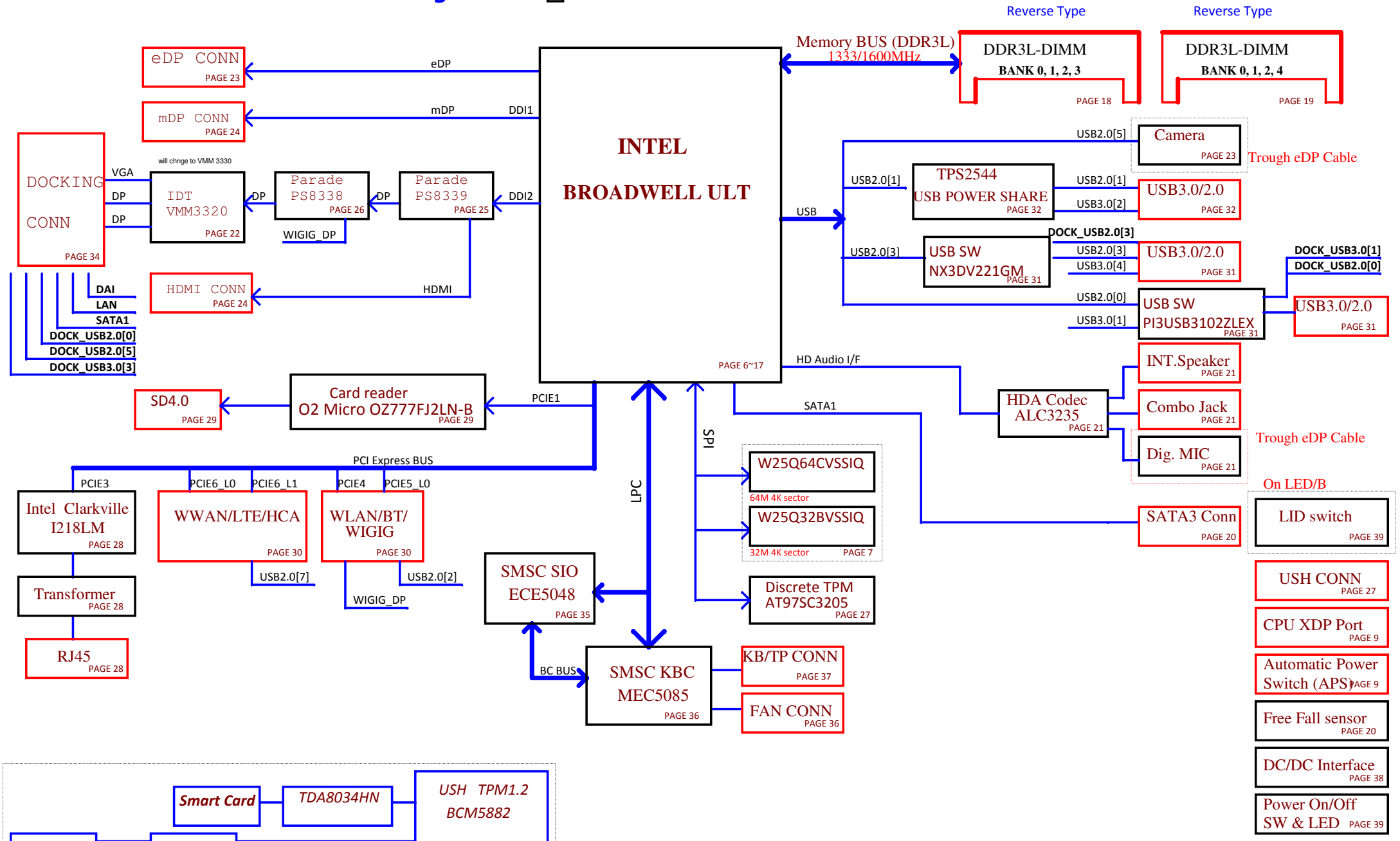
Size | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 1 of 56

Houston 12 - with Dock Block Diagram

: CONNECTOR

: IC



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Title: Block diagram

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE +1.5V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6	L3	SATA 0	JDOCK1
	L2	SATA 1	JSATA1 (HDD)
	L1	SATA 2	NA (SSD catch has dropped)
	L0	SATA 3	HCA (PCIE)

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA

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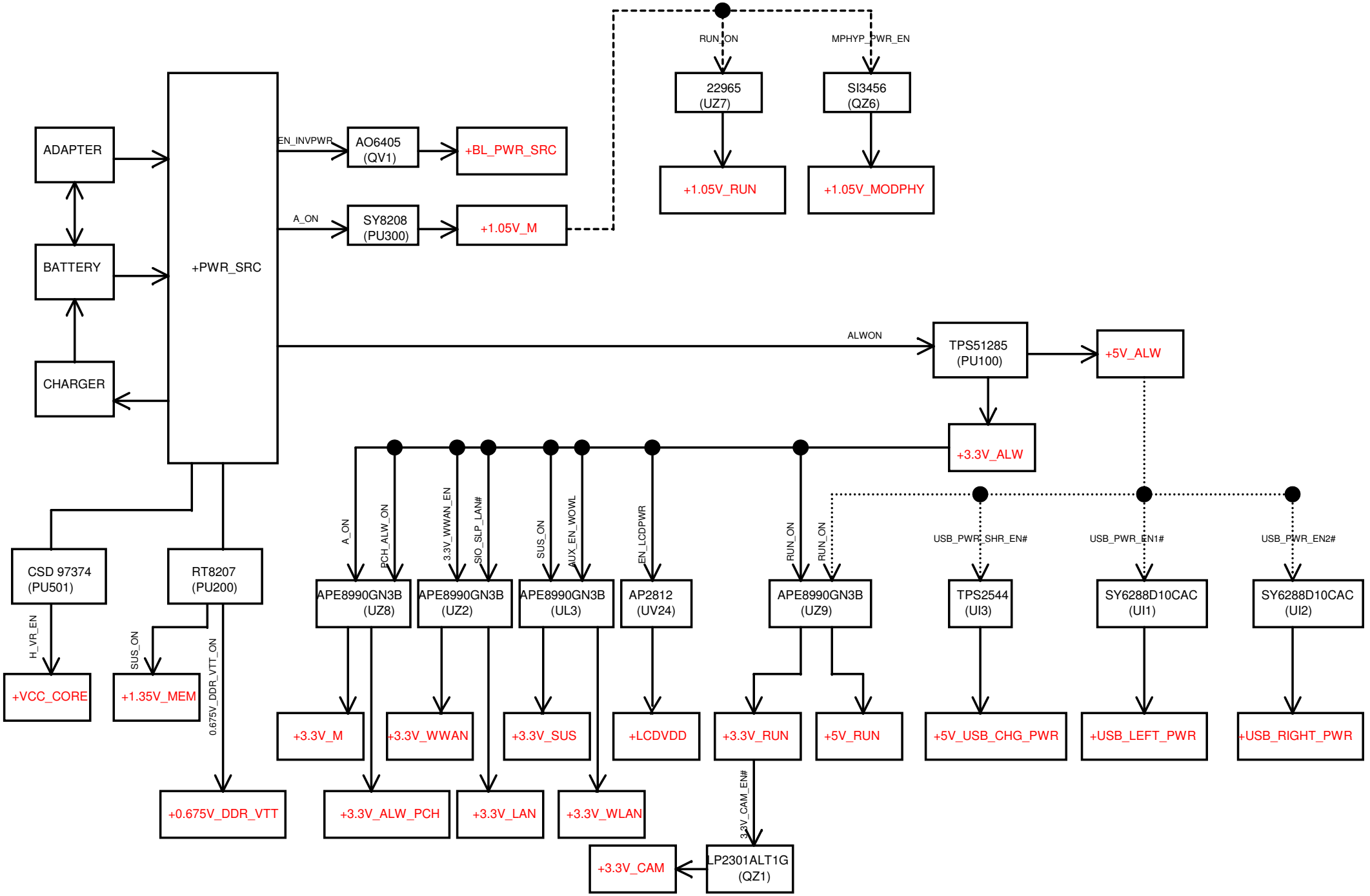

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Title	Power rails
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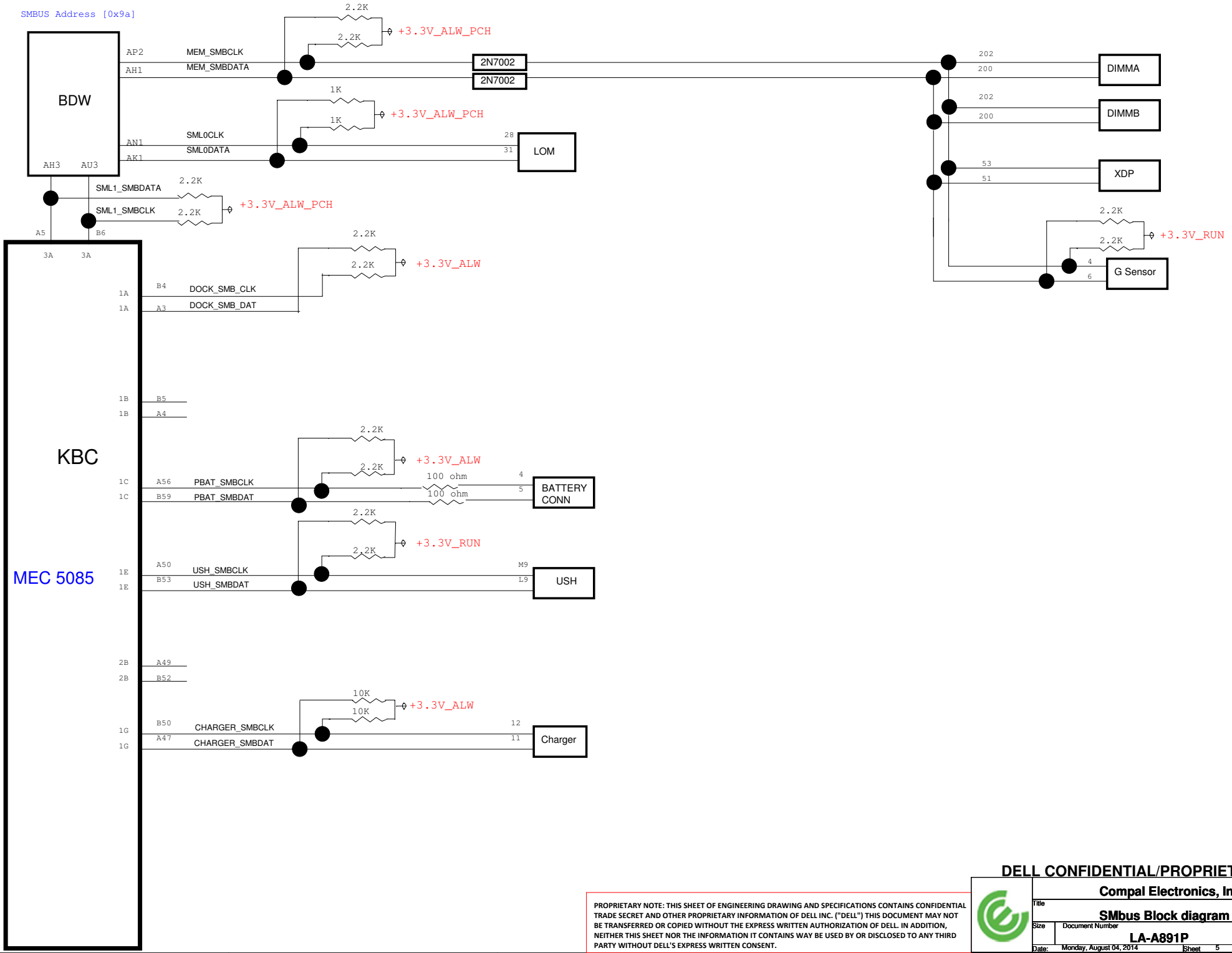

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Title: SMbus Block diagram

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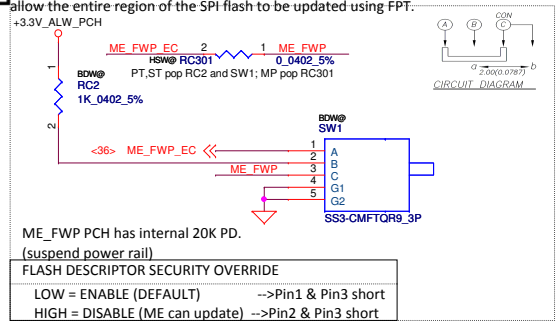
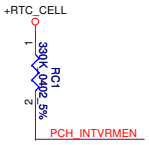
UMA SATA port

SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H12 Entry	NA	NA	
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H14U_En	NA	NA	
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H15D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H15U_En	NA	Express card	contact to Express card

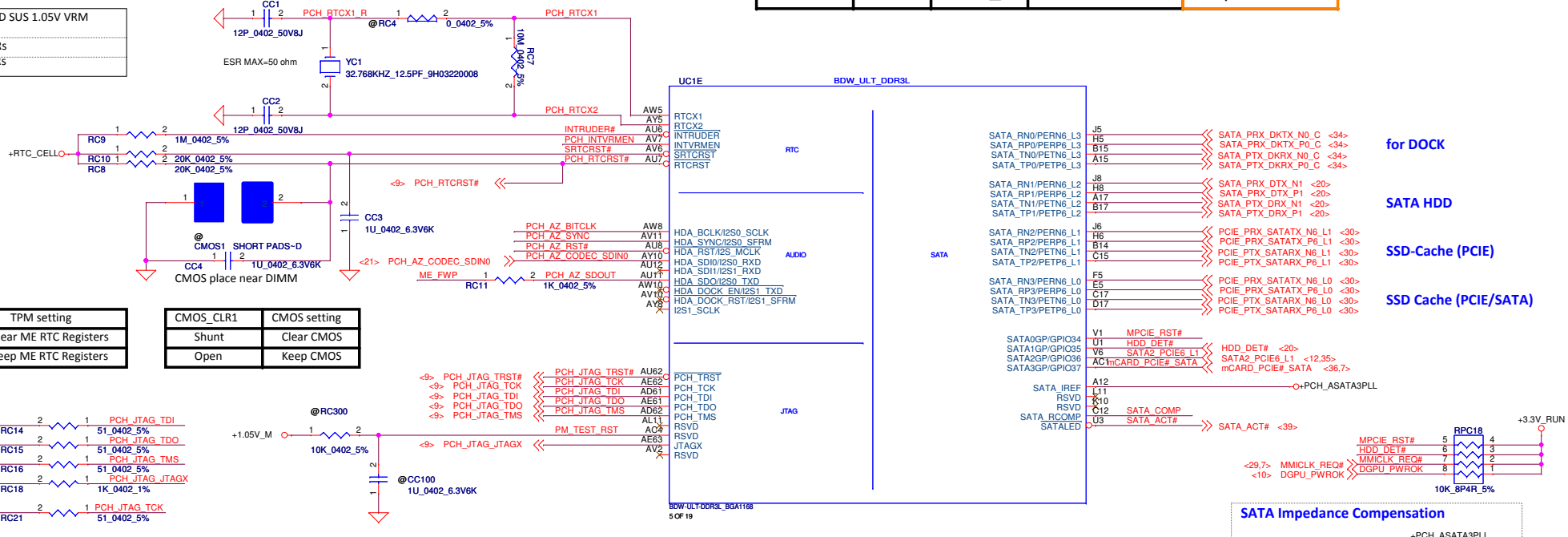
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

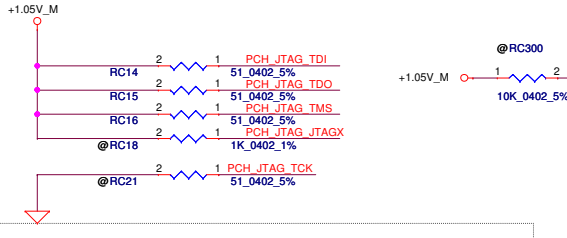


INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

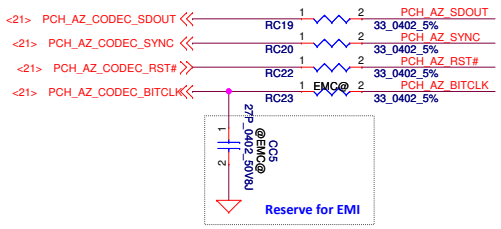


ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

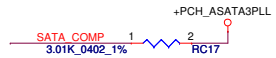
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



HDA for Codec



SATA Impedance Compensation



CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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Title: CPU (1/12)

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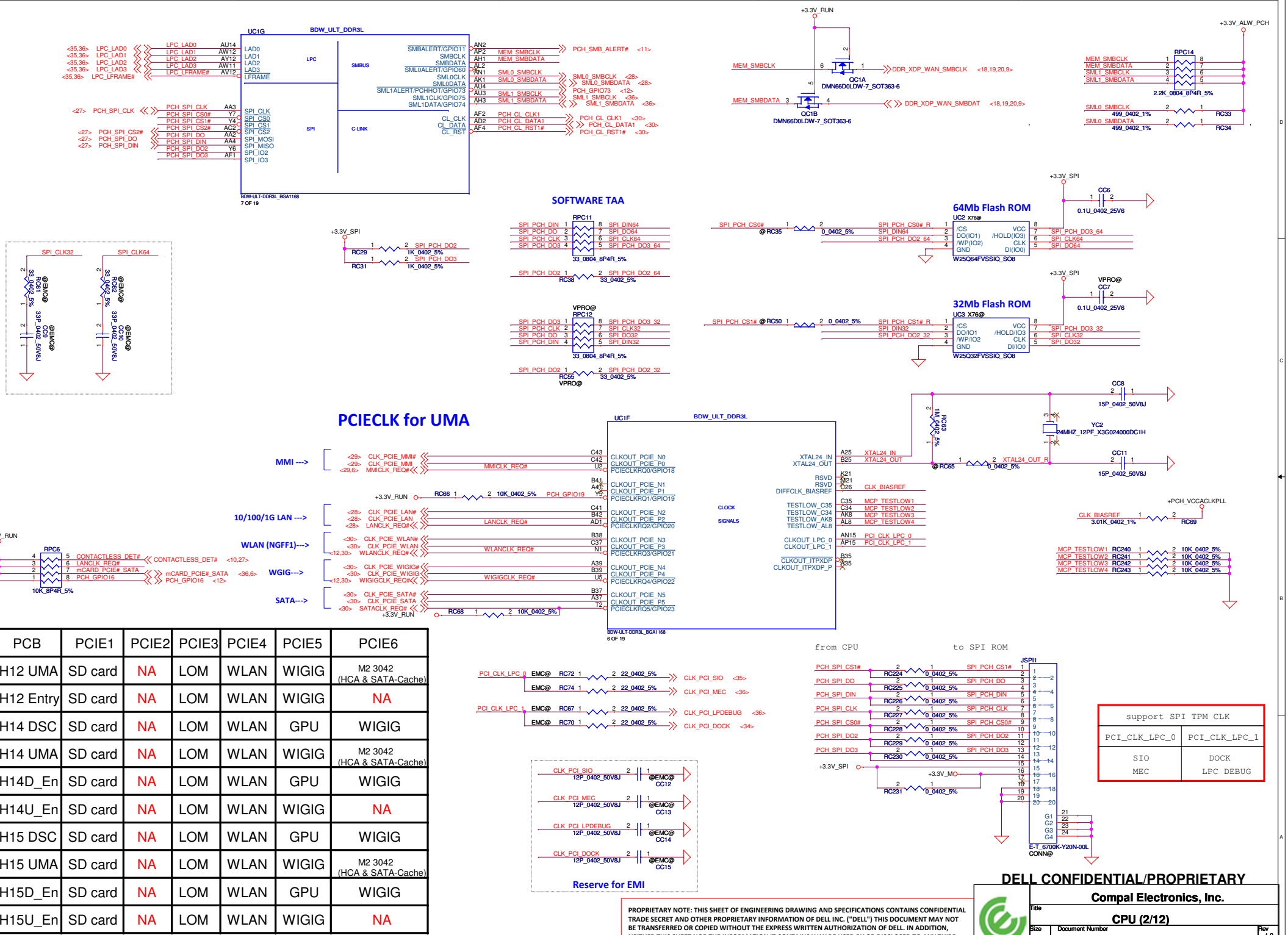

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

support SPI TPM CLK	
PCI_CLK_LPC_0	PCI_CLK_LPC_1
SIO	DOCK
MEC	LPC DEBUG

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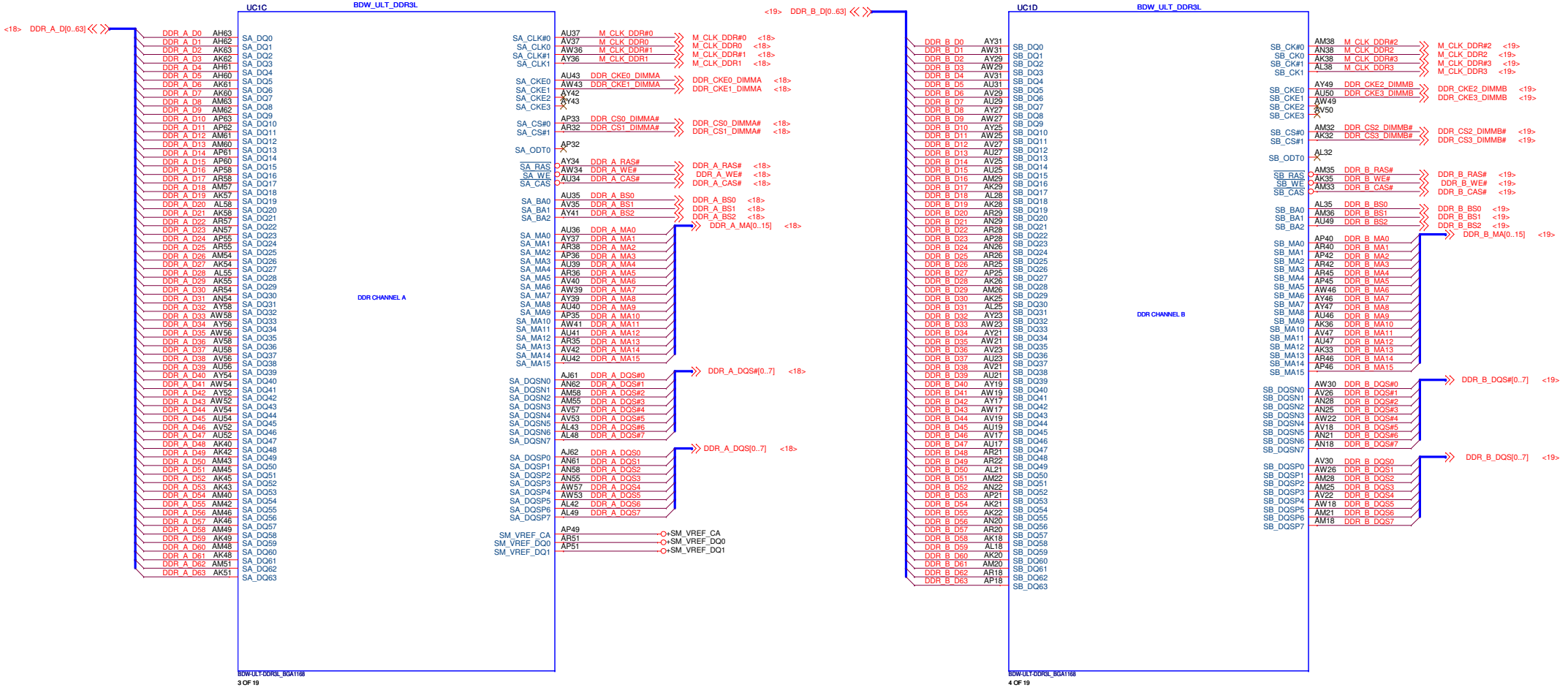

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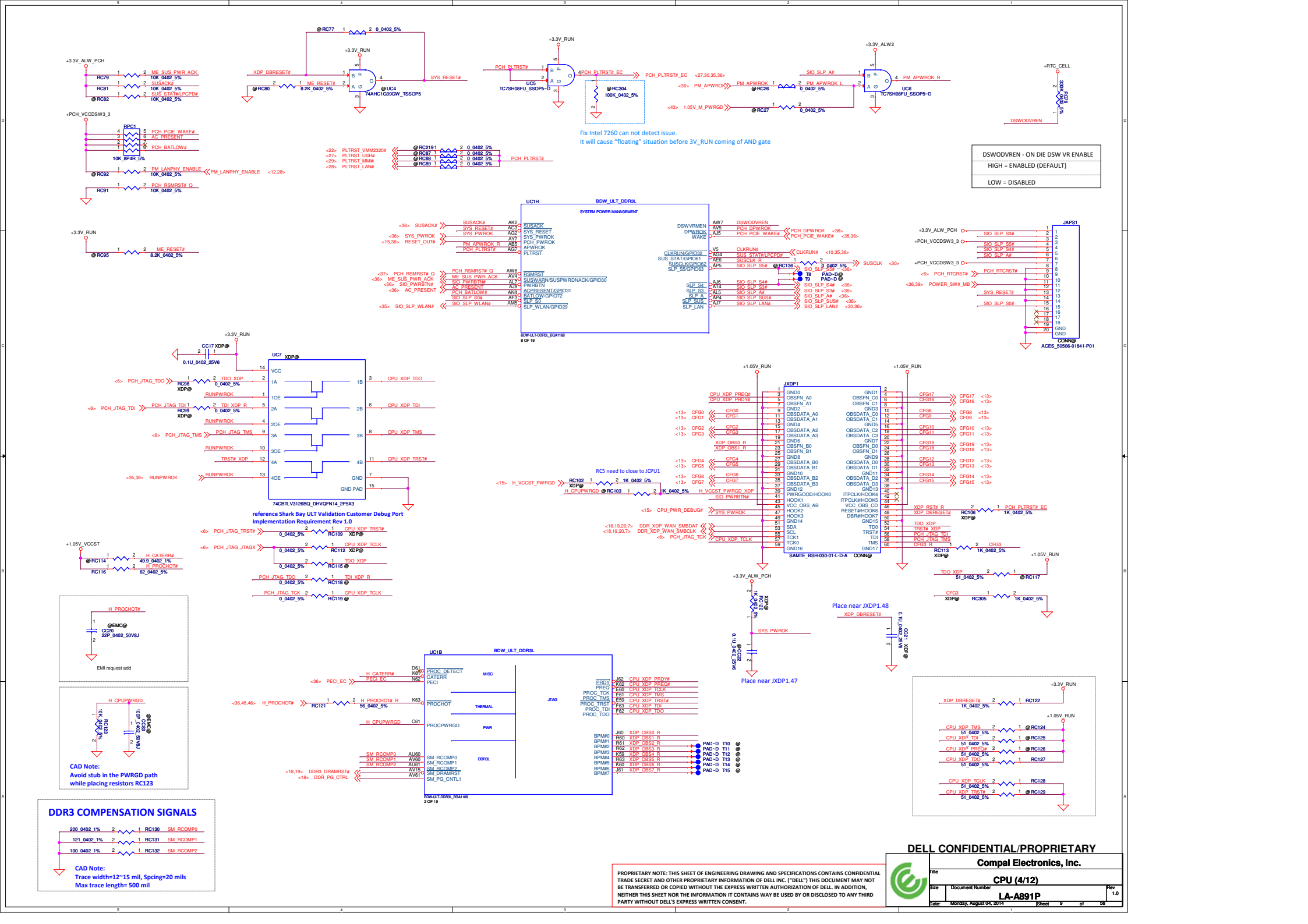
Fix Intel 7260 can not detect issue.
It will cause "floating" situation before 3V_RUN coming of AND gate
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
reference Shark Bay ULT Validation Customer Debug Port
Implementation Requirement Rev 1.0
RCS need to close to JCPU1
Place near JXDP1.48
Place near JXDP1.47
EMI request add
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC123
DDR3 COMPENSATION SIGNALS
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil
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CPU (4/12)
LA-A891P
Rev 1.0
Monday, August 04, 2014
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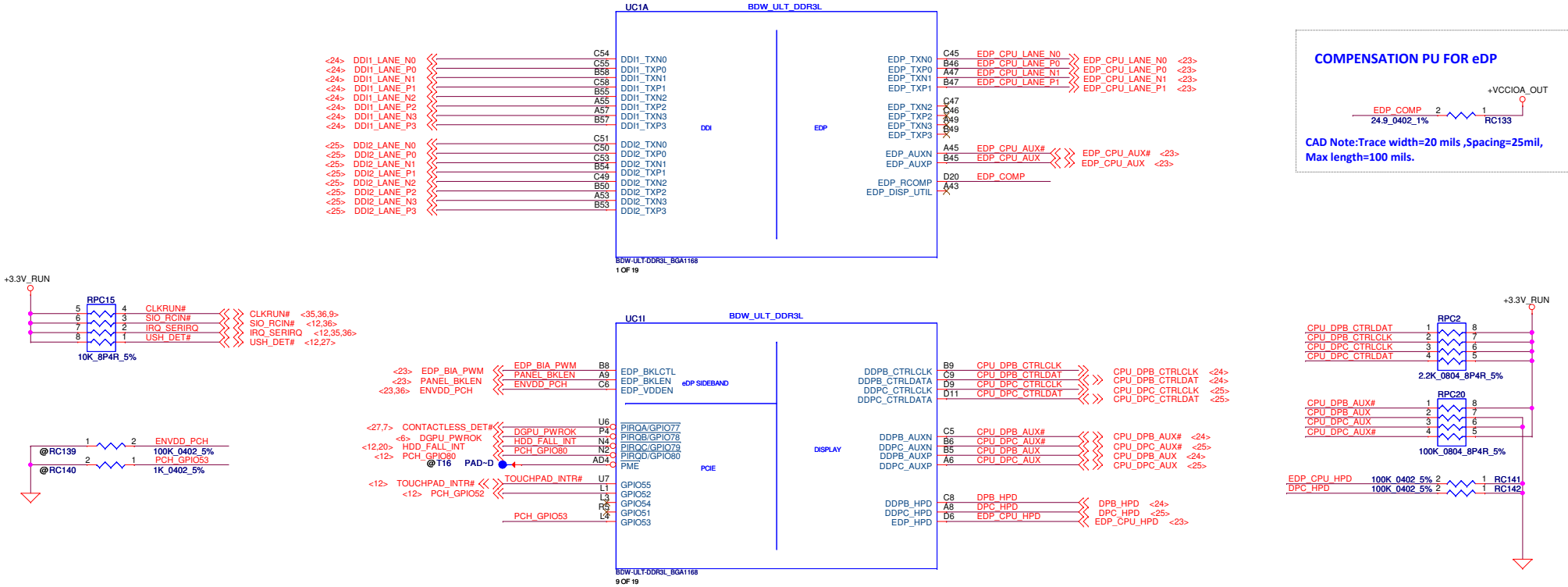

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Title	CPU (5/12)	
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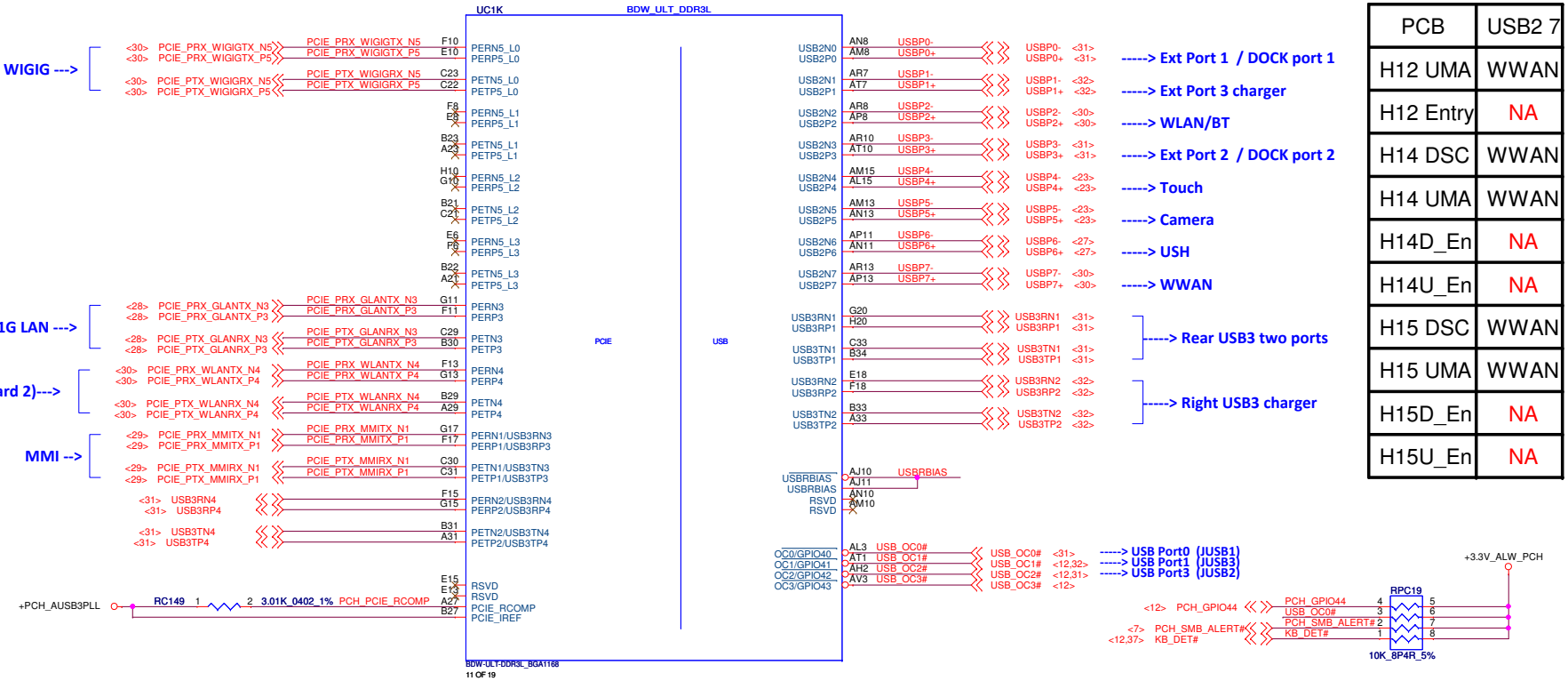
PCIE for UMA



PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	NA

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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Title: CPU (6/12)

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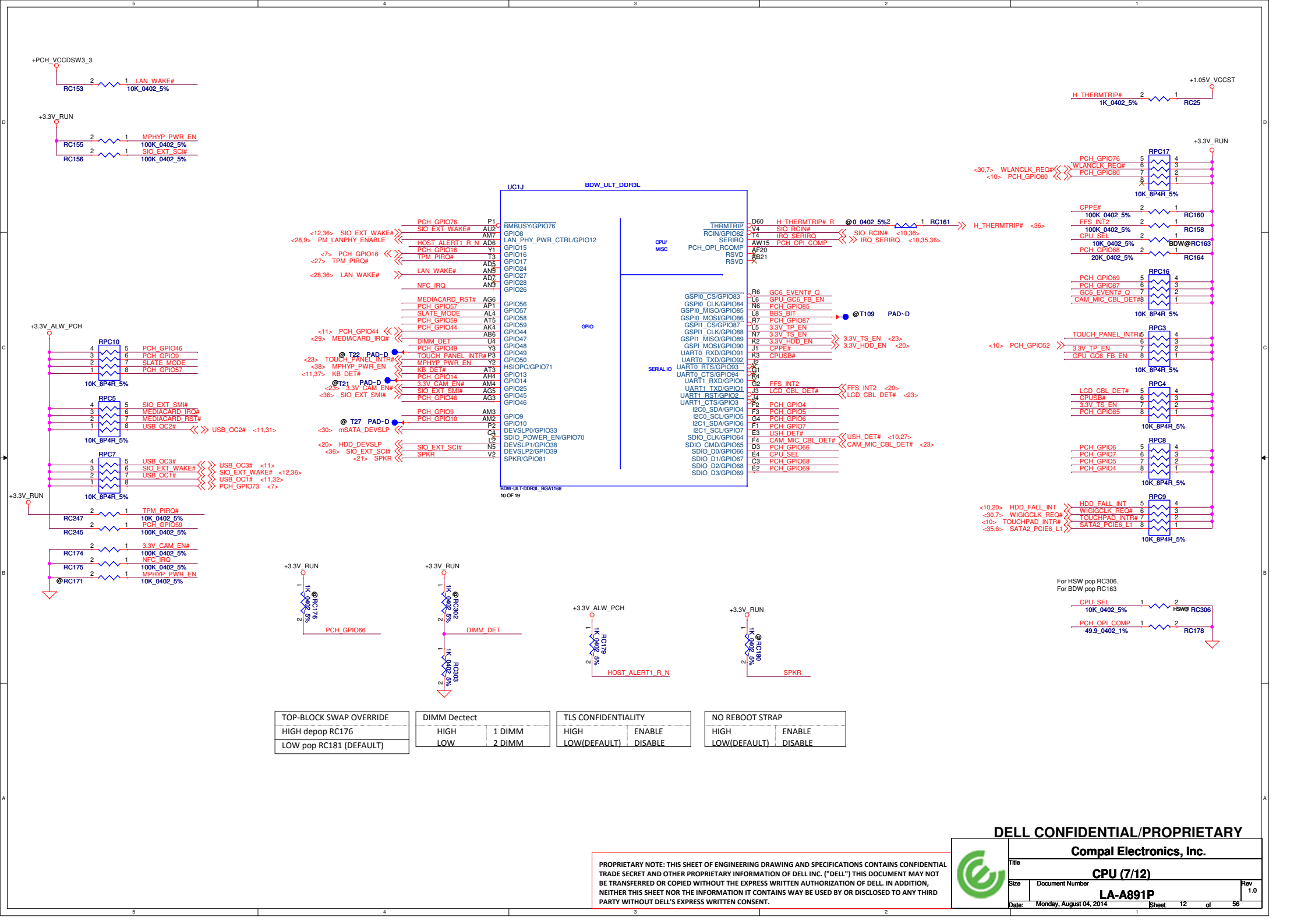

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Title: CPU (7/12)

Size | Document Number: LA-A891P | Rev: 1.0

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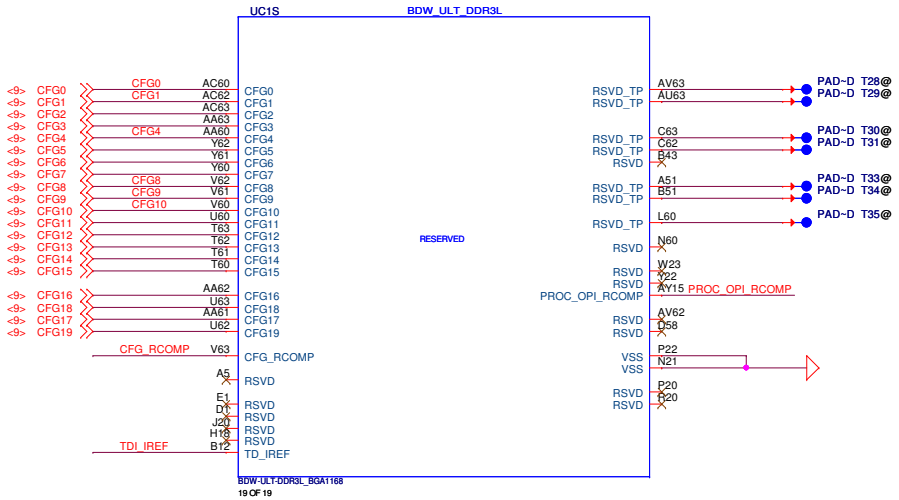
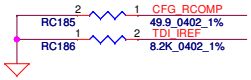
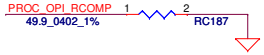
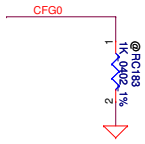
CFG STRAPS for CPU

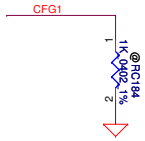




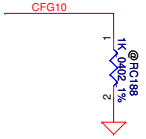


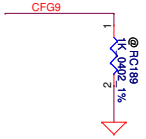


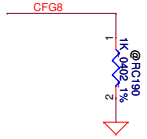
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

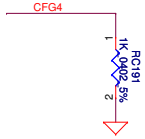


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: CPU (8/12)

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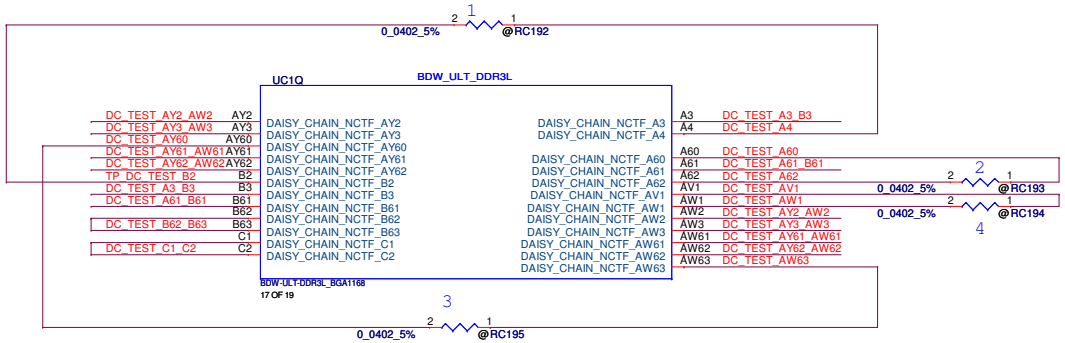


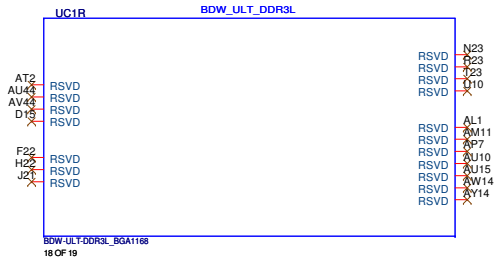
Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4

2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60

3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63

4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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Title: CPU (9/12)		
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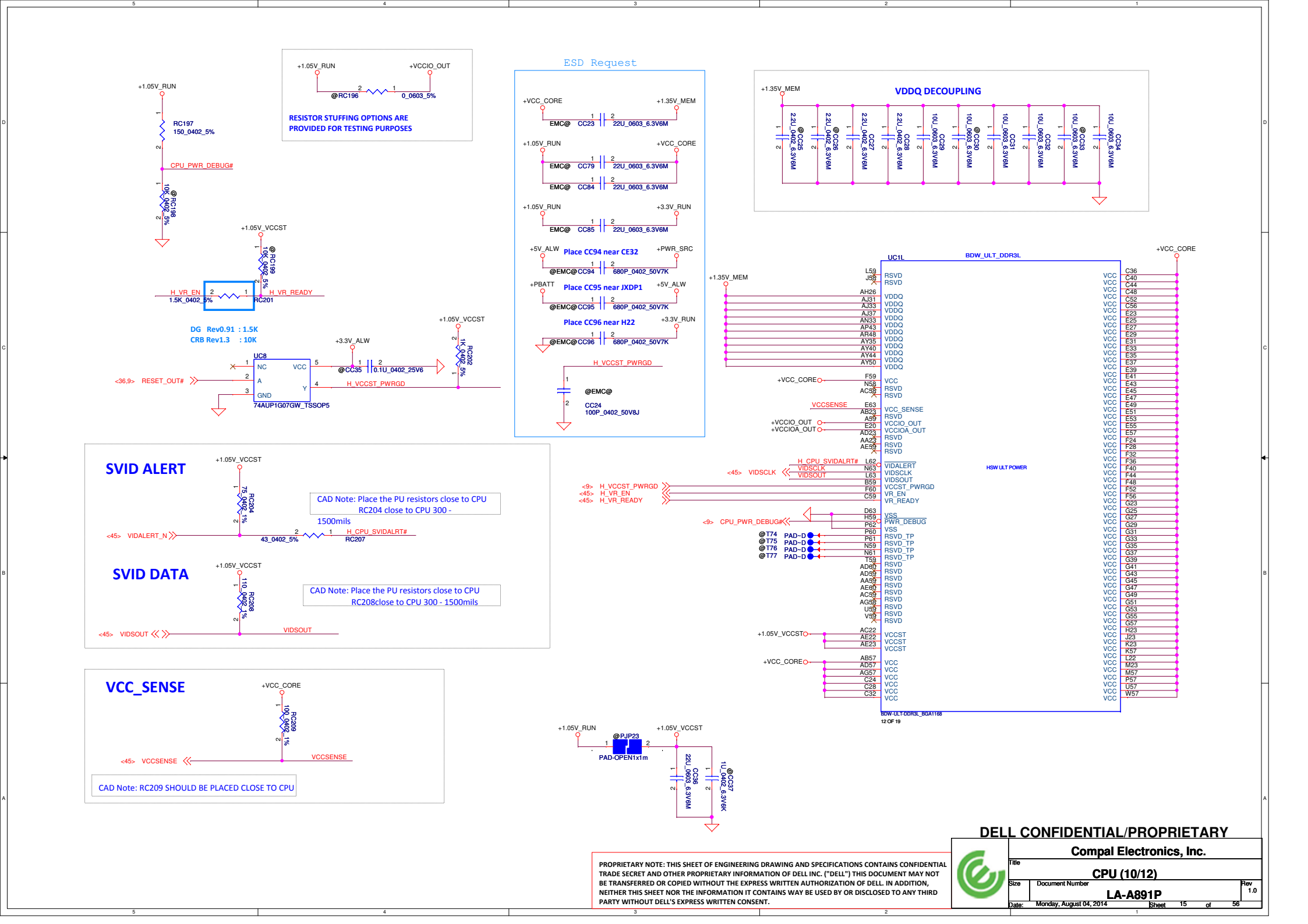
+1.05V_RUN
+VCCIO_OUT
@RC196
2
1
0_0603_5%
RESISTOR STUFFING OPTIONS ARE
PROVIDED FOR TESTING PURPOSES
ESD Request
+VCC_CORE
+1.35V_MEM
EMC@ CC23
22U_0603_6.3V6M
+1.05V_RUN
+VCC_CORE
EMC@ CC79
EMC@ CC84
+3.3V_RUN
EMC@ CC85
+5V_ALW
+PWR_SRC
Place CC94 near CE32
@EMC@CC94
680P_0402_50V7K
+PBATT
Place CC95 near JXDP1
@EMC@CC95
Place CC96 near H22
@EMC@CC96
H_VCCST_PWRGD
@EMC@
CC24
100P_0402_50V8J
VDDQ DECOUPLING
+1.35V_MEM
2.2U_0402_6.3V6M
@CC25
@CC26
CC27
CC28
10U_0603_6.3V6M
CC29
@CC30
CC31
CC32
@CC33
CC34
RC197
150_0402_5%
CPU_PWR_DEBUG#
10K_0402_5%
@RC198
+1.05V_VCCST
10K_0402_5%
@RC199
H_VR_EN
1.5K_0402_5%
RC200
H_VR_READY
RC201
DG Rev0.91 : 1.5K
CRB Rev1.3 : 10K
+3.3V_ALW
+1.05V_VCCST
1K_0402_5%
RC202
UC8
NC
VCC
A
Y
GND
74AUP1G07GW_TSSOP5
<36,9> RESET_OUT#
@CC35
0.1U_0402_25V6
H_VCCST_PWRGD
SVID ALERT
+1.05V_VCCST
75_0402_1%
RC204
CAD Note: Place the PU resistors close to CPU
RC204 close to CPU 300 -
1500mils
<45> VIDALERT_N
43_0402_5%
H_CPU_SVIDALRT#
RC207
SVID DATA
+1.05V_VCCST
110_0402_1%
RC208
CAD Note: Place the PU resistors close to CPU
RC208close to CPU 300 - 1500mils
<45> VIDSOUT
VIDSOUT
VCC_SENSE
+VCC_CORE
100_0402_1%
RC209
<45> VCCSENSE
VCCSENSE
CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU
UC1L
BDW_ULT_DDR3L
HSW ULT POWER
BDW-ULT-DDR3L_BGA1168
12 OF 19
+1.35V_MEM
+VCC_CORE
VCCSENSE
+VCCIO_OUT
+VCCIOA_OUT
H_CPU_SVIDALRT#
<45> VIDSCLK
<9> H_VCCST_PWRGD
<45> H_VR_EN
<45> H_VR_READY
<9> CPU_PWR_DEBUG#
@T74 PAD~D
@T75 PAD~D
@T76 PAD~D
@T77 PAD~D
+1.05V_VCCST
+VCC_CORE
+1.05V_RUN
+1.05V_VCCST
@PJP23
PAD-OPEN1x1m
CC36
22U_0603_6.3V6M
@CC37
10U_0402_6.3V6K
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Compal Electronics, Inc.
Title
CPU (10/12)
Size
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Rev
1.0
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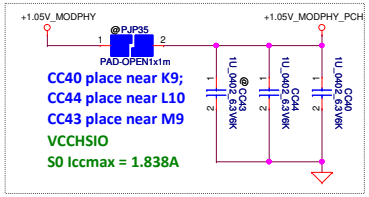

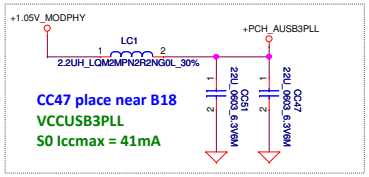

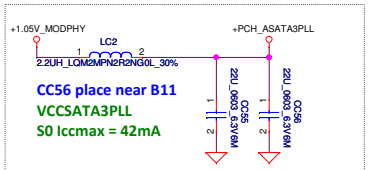

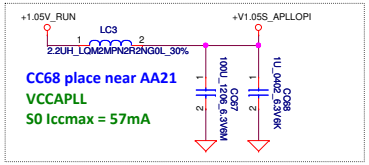

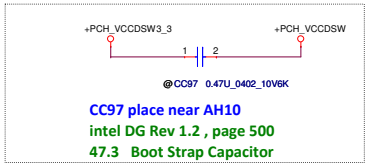

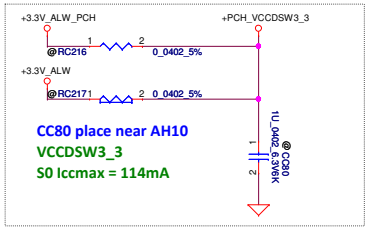

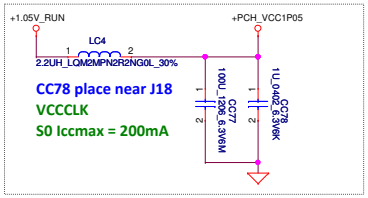

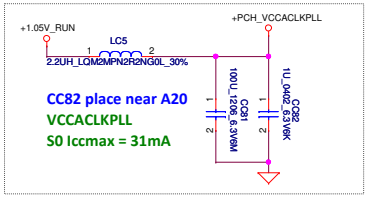

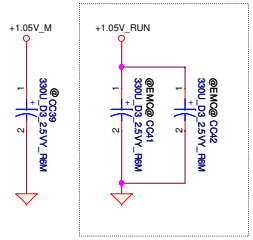

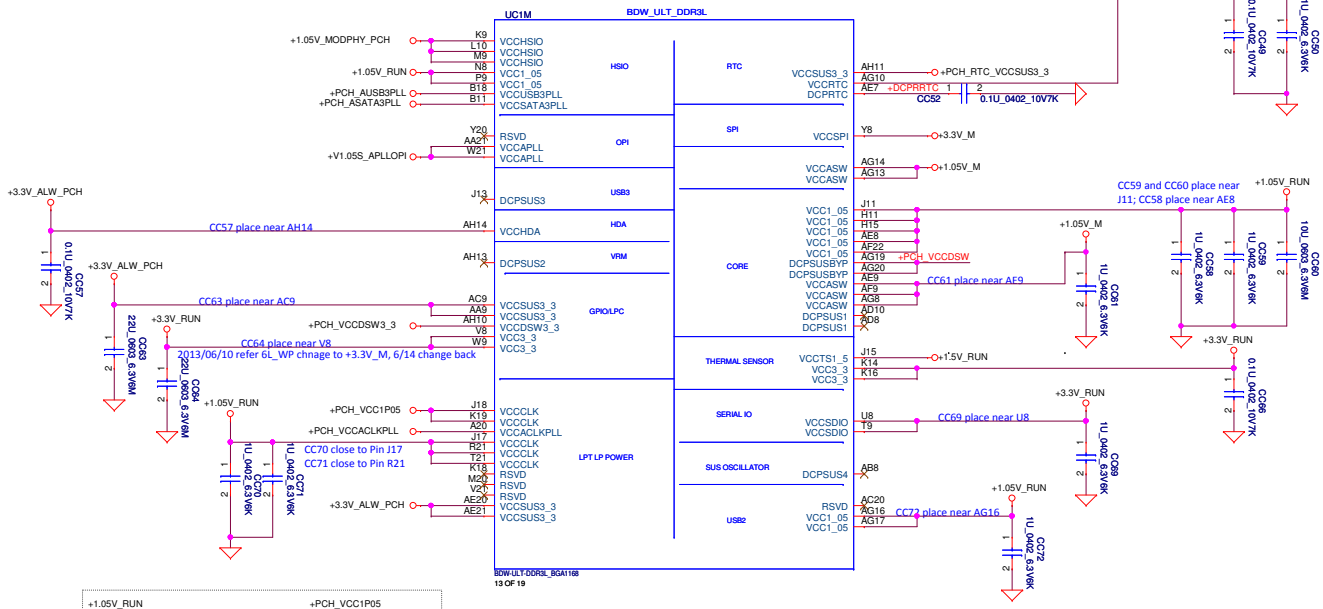

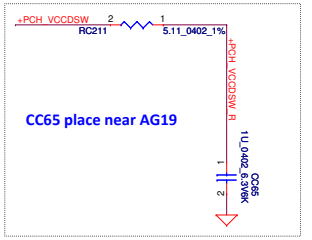

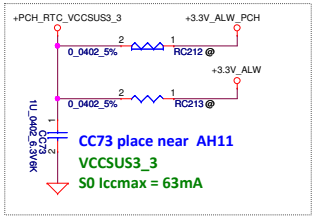

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

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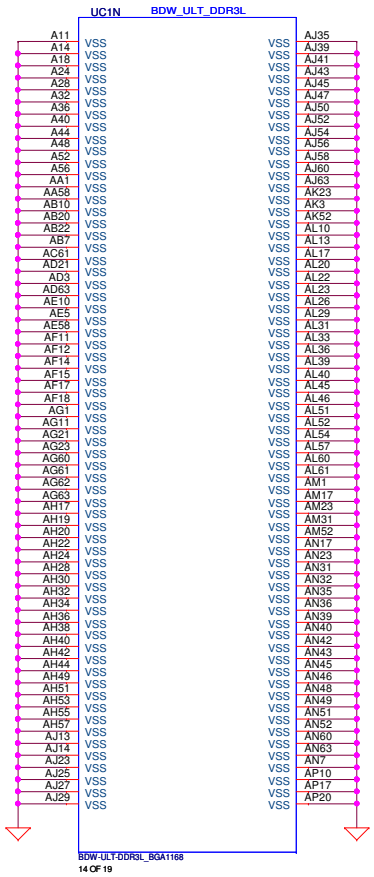

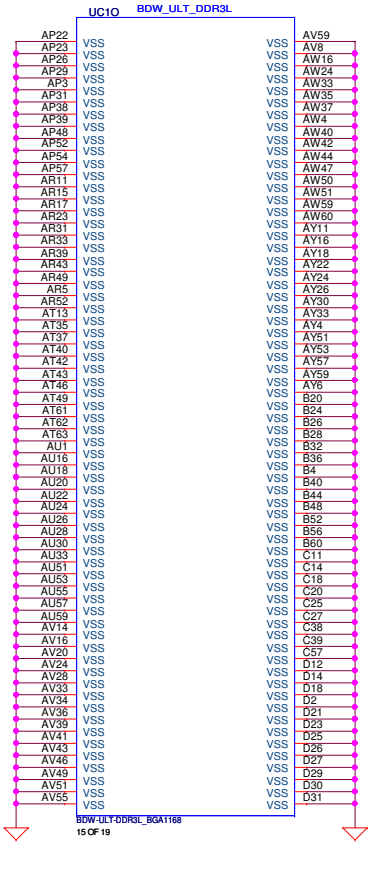

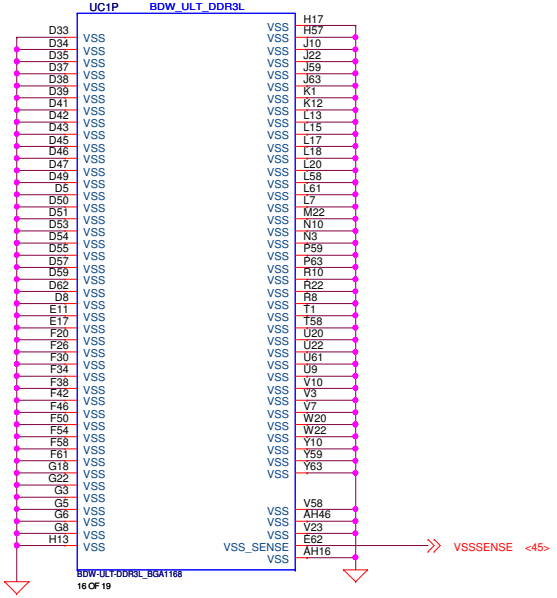

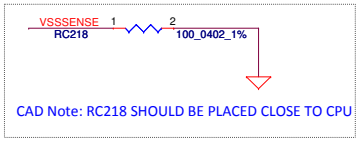

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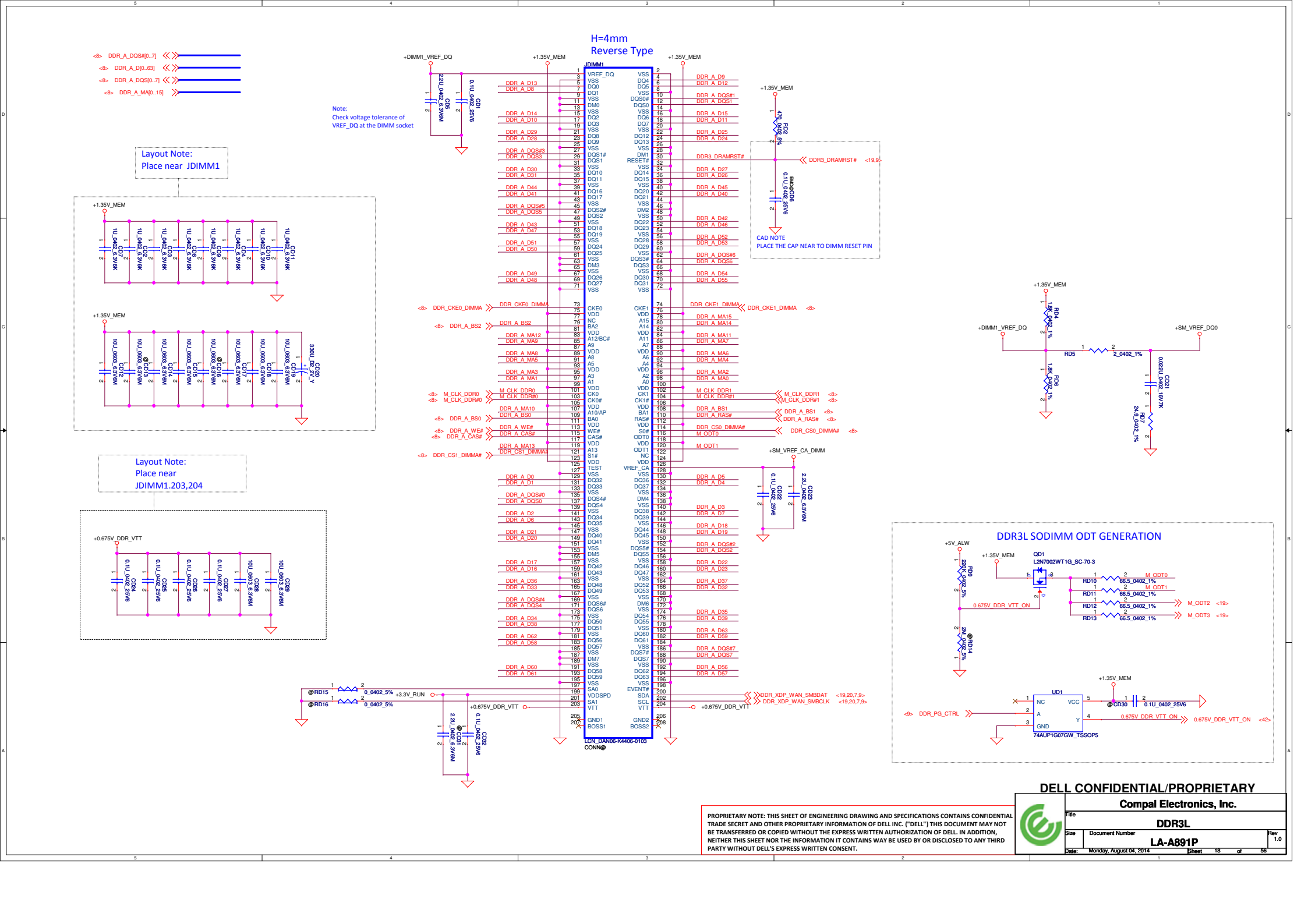
H=4mm
Reverse Type
JDIMM1
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMM1
Layout Note:
Place near
JDIMM1.203,204
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN
DDR3L SODIMM ODT GENERATION
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Size
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1.0
Date: Monday, August 04, 2014
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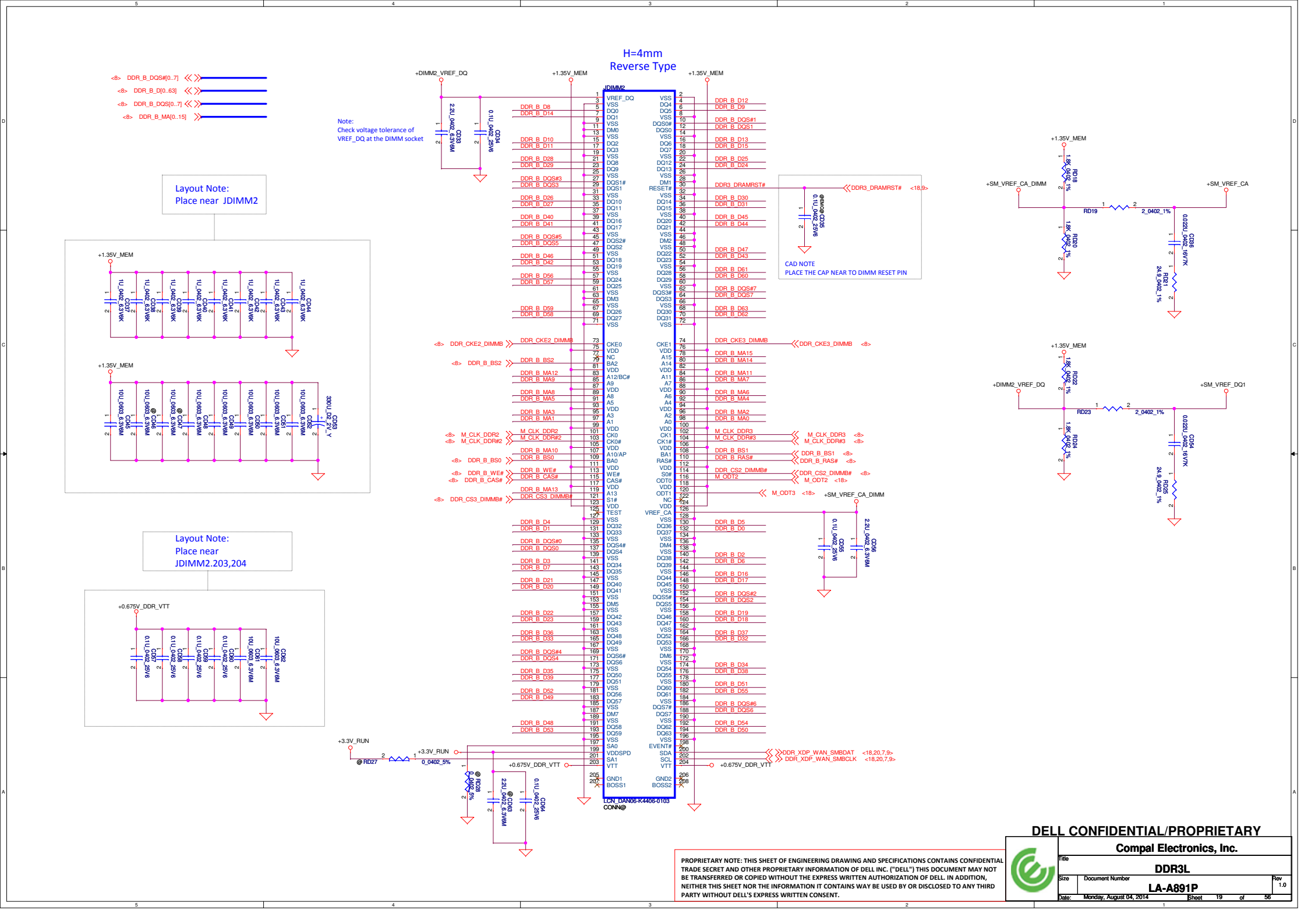

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Title: DDR3L

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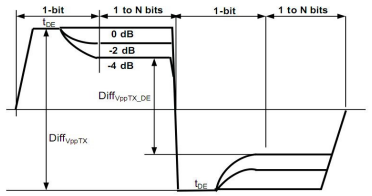


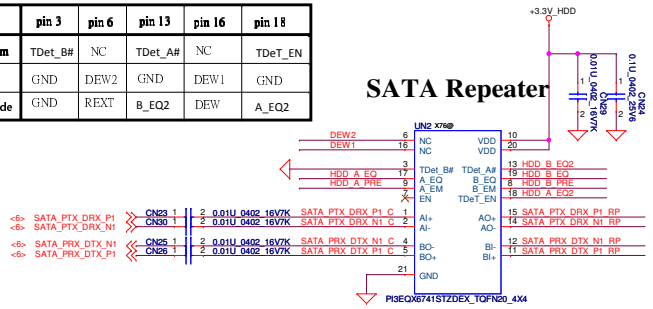
De-emphsis= 20 * log(V Diff vppTX / V Diff vppTX_DE)

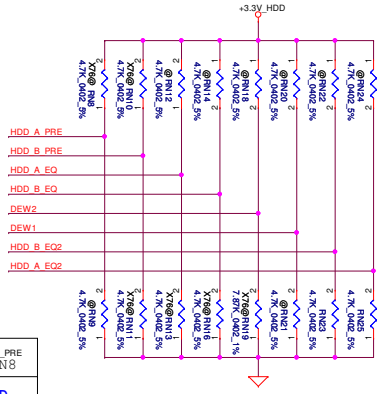
	REXT	Diff vppTX	Pre-emphsis	Diff vpp TX_Pre
Pericom	NA	600mV	0dB	600mV
		600mV	-1.5dB	713mV
	REXT	Diff vppTX	De-emphsis	Diff vpp TX_DE
TI	NA		0dB	550mV
		to be confirmed	-4dB	630mV
			-2dB	830mV
Parade	4.99K	1200mV	0dB	1200mV
		1200mV	-1.5dB	1009mV
		1200mV	-3.5dB	802mV
	6.04K	1100mV	0dB	1100mV
		1100mV	-1.5dB	925mV
		1100mV	-3.5dB	735mV
	7.5K	1000mV	0dB	1000mV
		1000mV	-1.5dB	841mV
		1000mV	-3.5dB	668mV
	10K	900mV	0dB	900mV
		900mV	-1.5dB	757mV
		900mV	-3.5dB	602mV
	15K	800mV	0dB	800mV
		800mV	-1.5dB	673mV
		800mV	-3.5dB	534mV

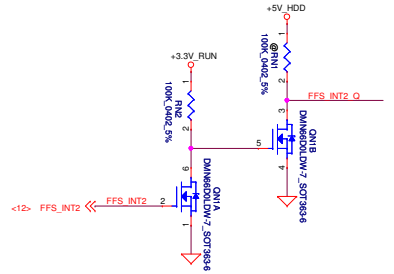
to be confirmed

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater



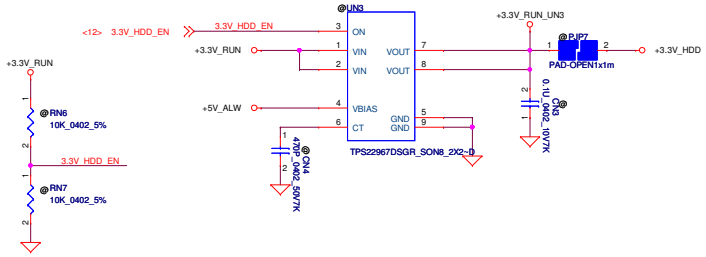


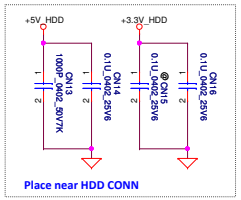


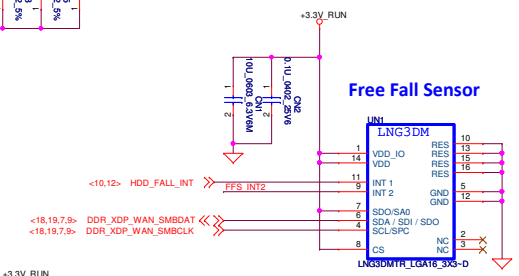
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	NC	PD (RN16)	PD (RN25)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN25)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN25)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

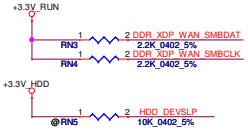
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	A_EQ2 A_EQ PIN18 PIN17 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	B_EQ2 B_EQ PIN13 PIN19 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 M 1	A_EM 0dB -3.5dB -1.5dB	B_EM 0dB -3.5dB -1.5dB

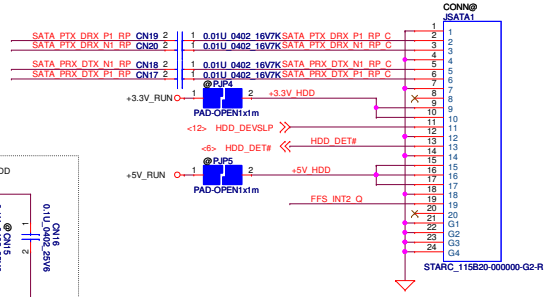
* red color is current setting











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Compal Electronics, Inc.

Title: HDD CONN

Size: | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 20 of 56

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1 — ACES_50279-0040N-001

Close to UA1

Close to UA1 pin6

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

Digital Mic

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place CA29 close to Codec

Place CA12 & CA13 close to Audio Jack

Universal Jack

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC
Global Headset

Normal Open

CIS Link OK

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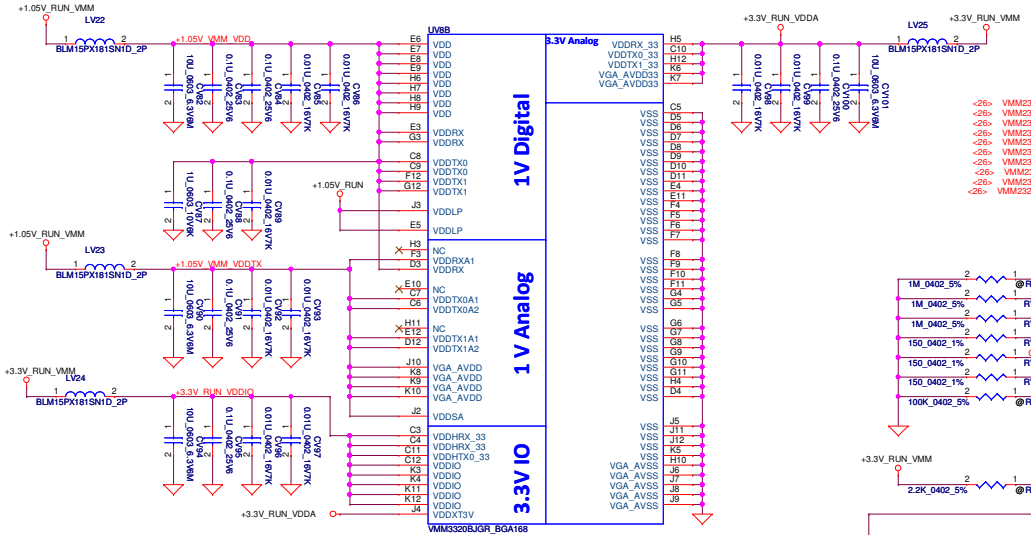
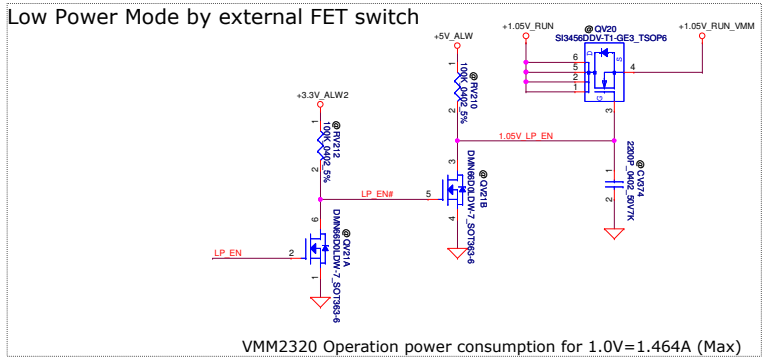
Compal Electronics, Inc.

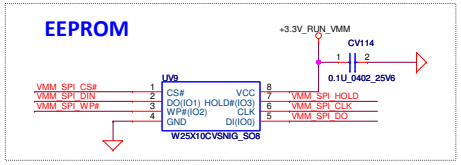
Title: Codec ALC3235

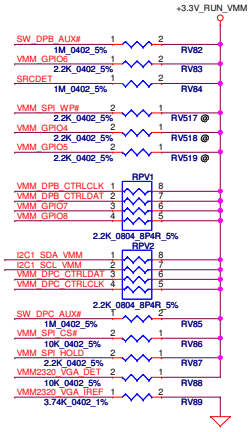
Size: — Document Number: LA-A891P — Rev: 1.0

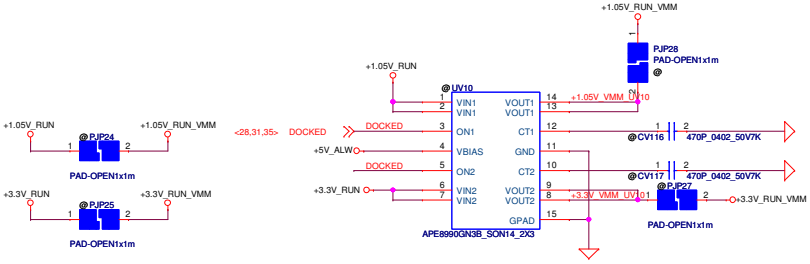
Date: Monday, August 04, 2014 — Sheet 21 of 56











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Compal Electronics, Inc.	
Title	DP 1.2 MST HUB
Size	Document Number: LA-A891P
Rev	1.0
Date:	Monday, August 04, 2014
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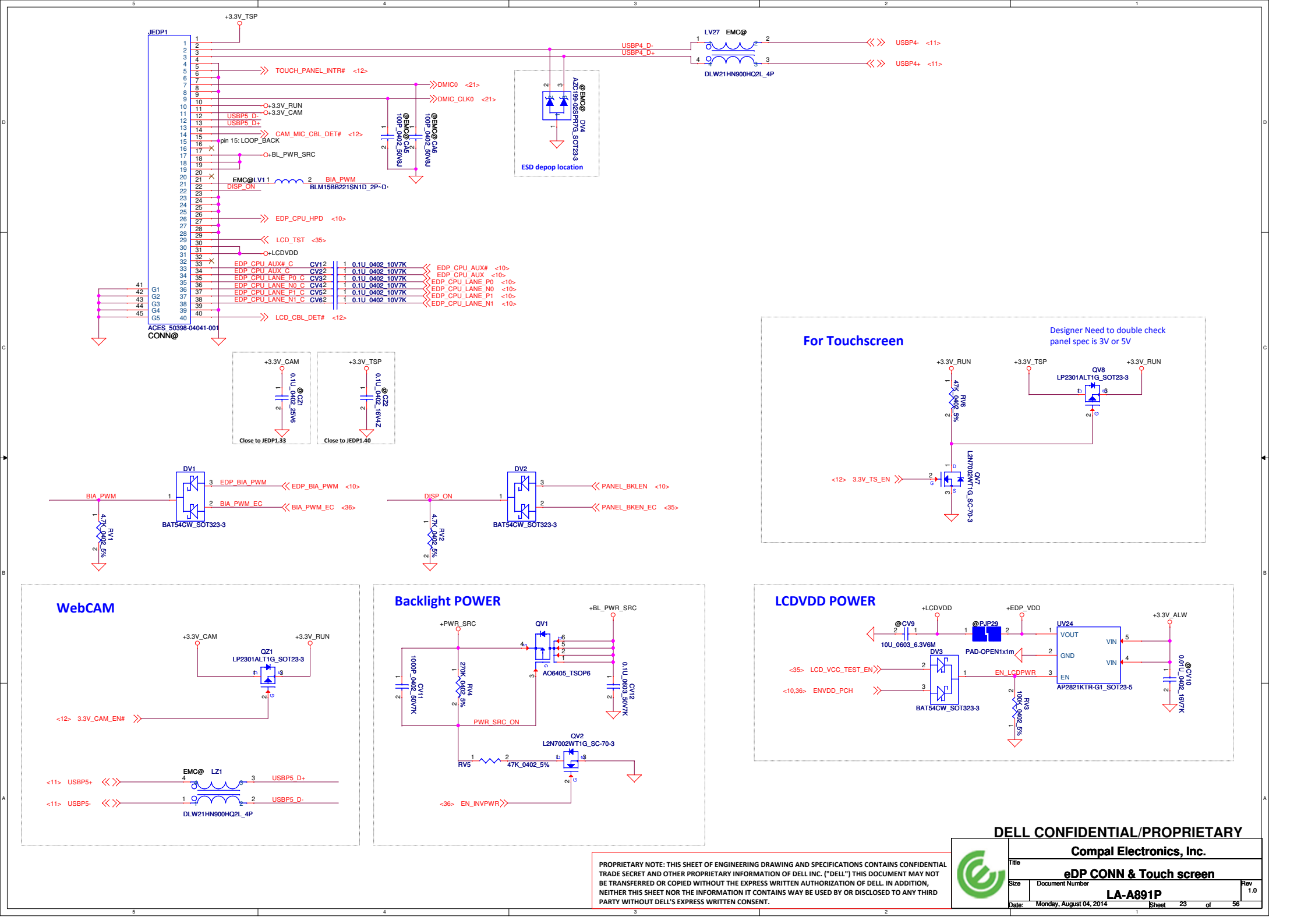

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Compal Electronics, Inc.	
Title	eDP CONN & Touch screen
Size	Document Number: LA-A891P
Rev	1.0
Date:	Monday, August 04, 2014
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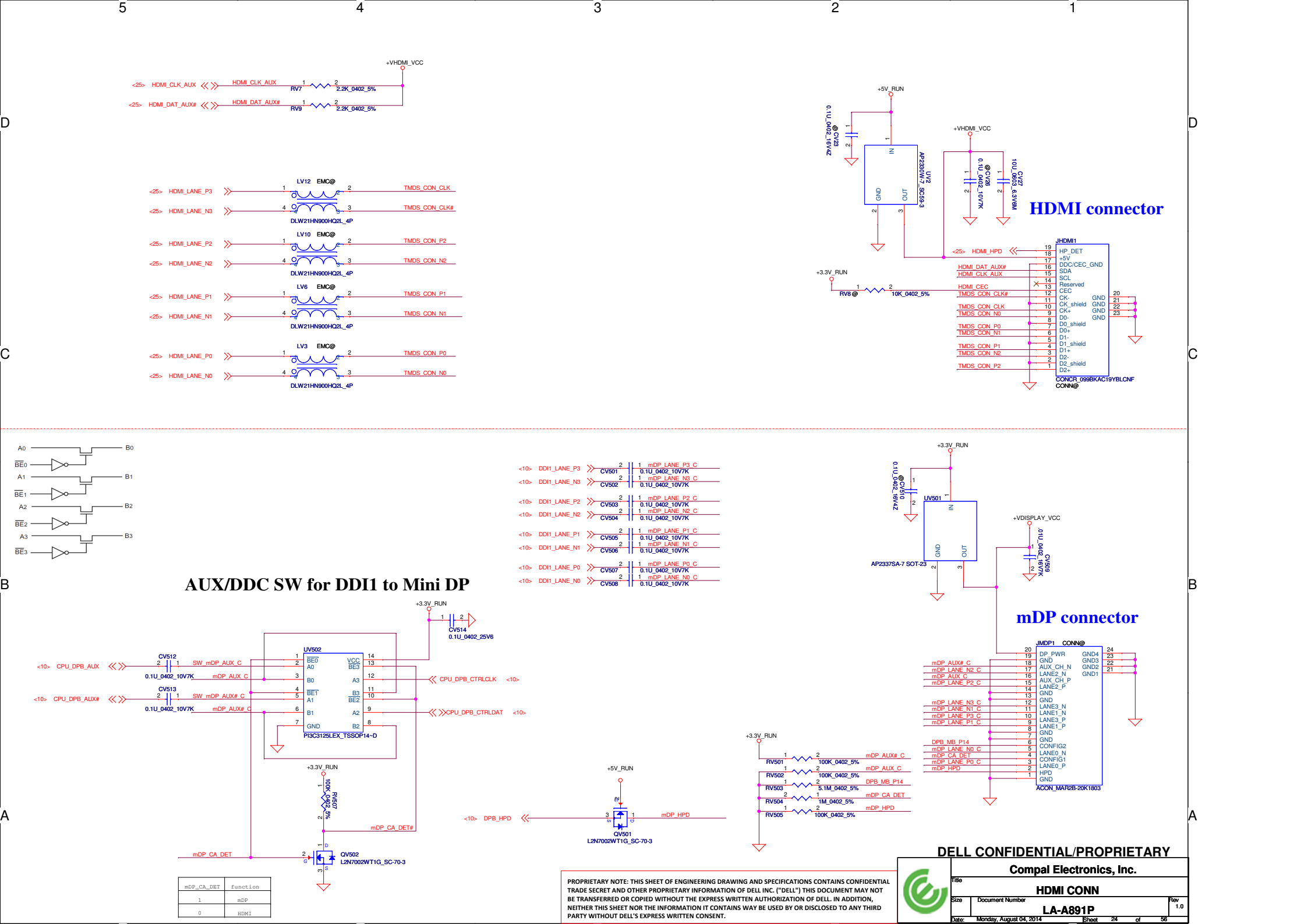

mDP_CA_DET	function
1	mDP
0	HDMI

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Compal Electronics, Inc.

Title: HDMI CONN

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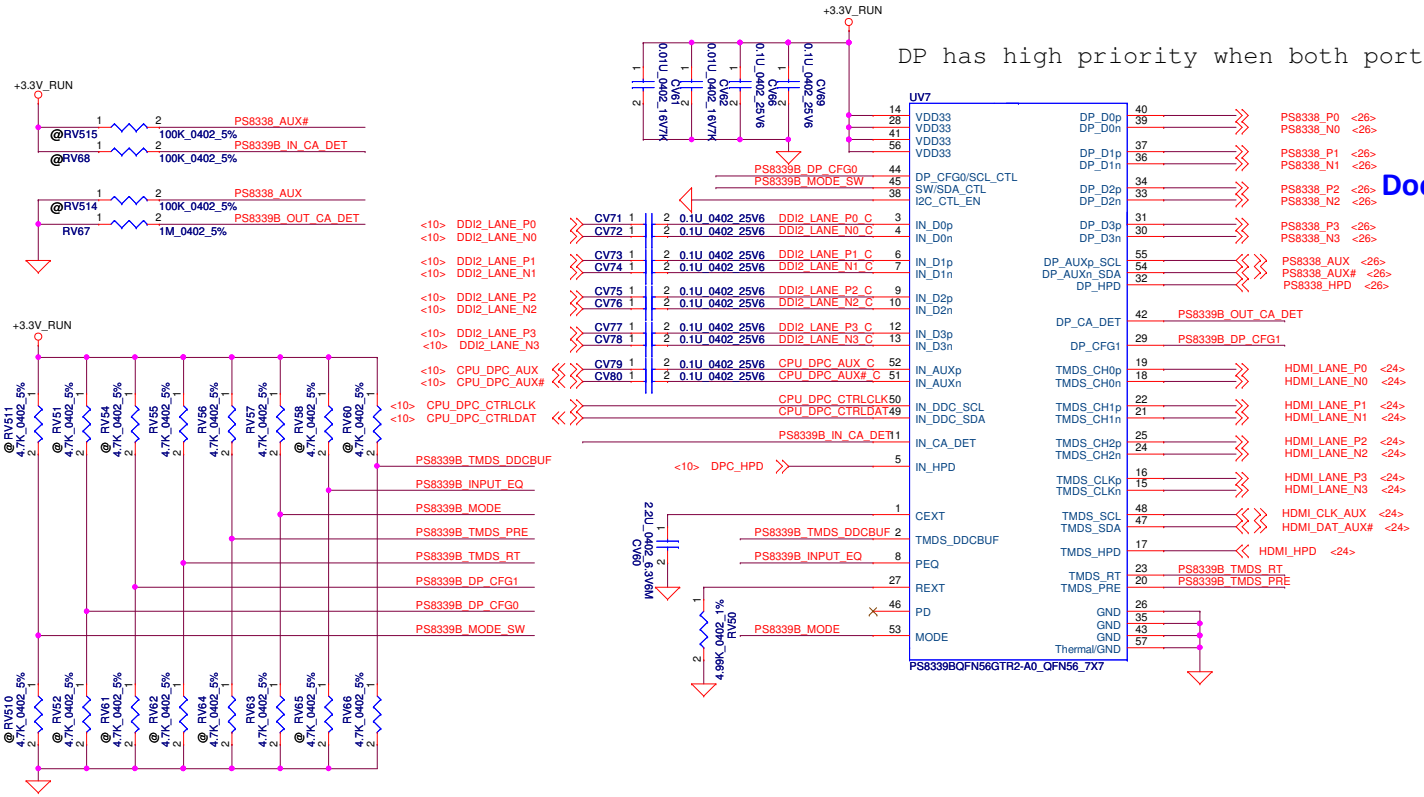
PCB	DP SWITCH
H12 UMA	PS8338+PS8339
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338



MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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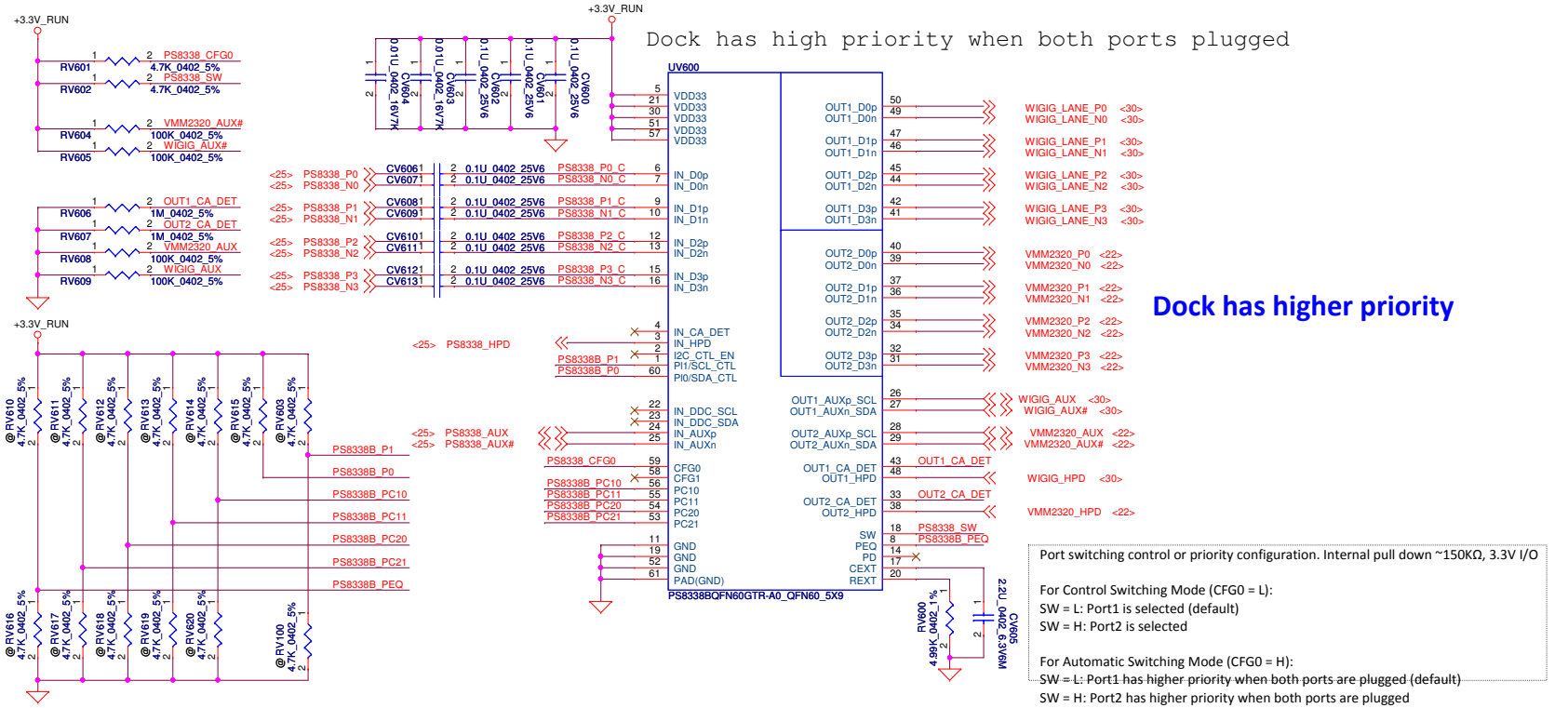
Compal Electronics, Inc.

Title: DP SW

Size | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 25 of 56

PCB	DP SWITCH
H12 UMA	PS8338+PS8339
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338

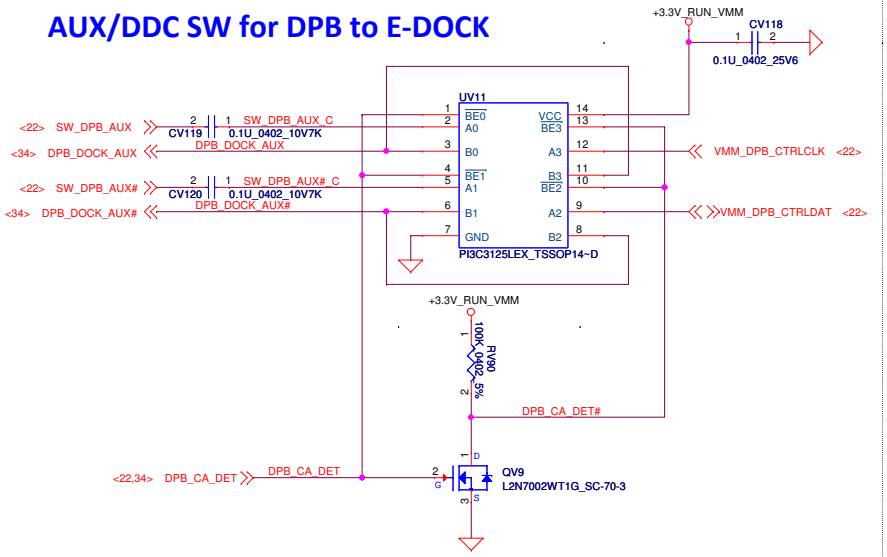


Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O

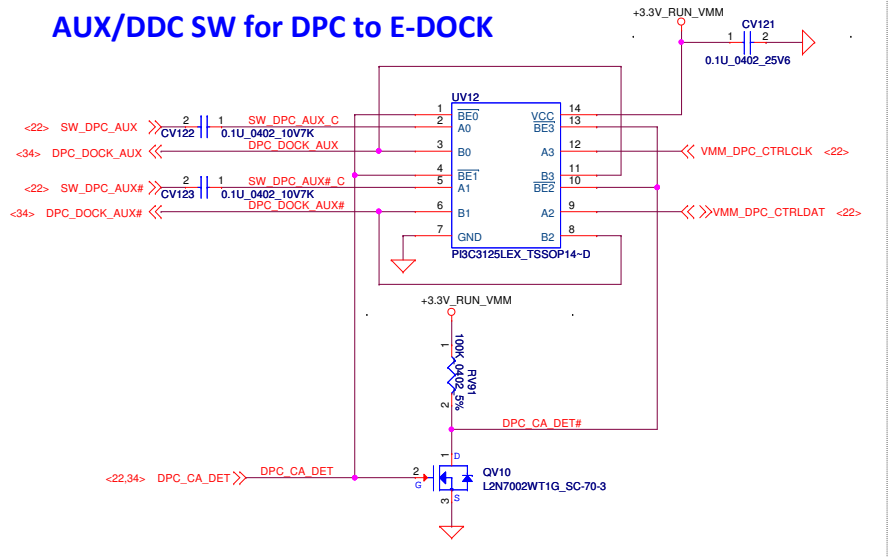
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

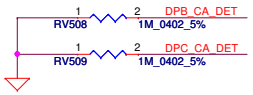
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

AUX/DDC SW for DPB to E-DOCK



AUX/DDC SW for DPC to E-DOCK





	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

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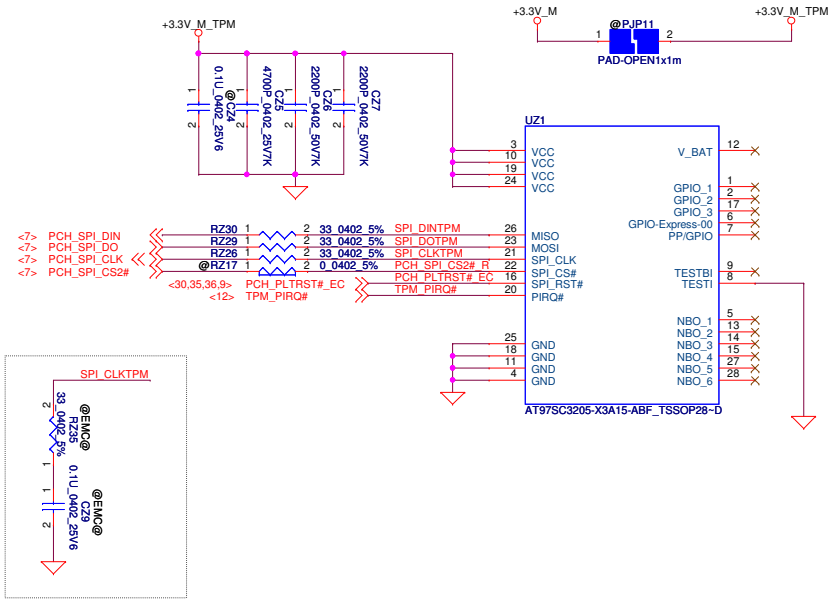
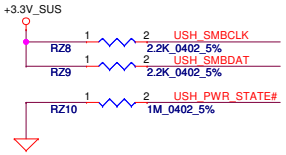
Compal Electronics, Inc.

Title: DP SW

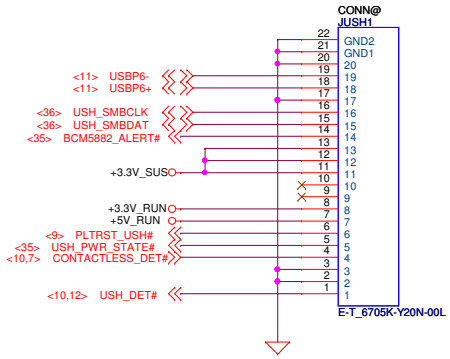
Size | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 26 of 56





USH CONN



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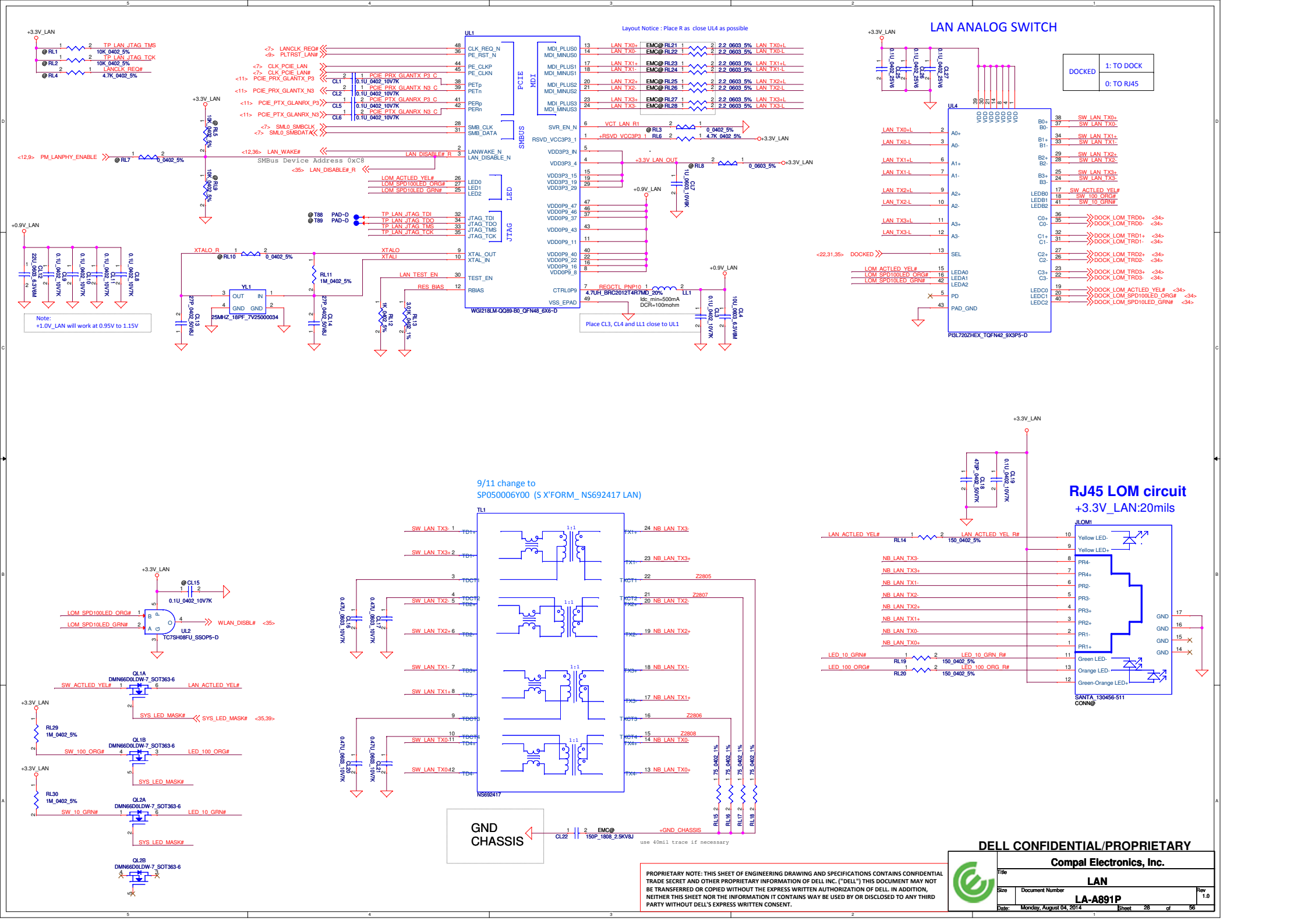
Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 27 of 56


LAN ANALOG SWITCH
Layout Notice : Place R as close UL4 as possible
UL1
WGI218LM-QQ89-B0_QFN48_6X6-D
UL4
PI3L720ZHEX_TQFN42_9X3P5-D
DOCKED
1: TO DOCK
0: TO RJ45
SMBus Device Address 0xC8
Note:
+1.0V_LAN will work at 0.95V to 1.15V
Place CL3, CL4 and LL1 close to UL1
9/11 change to
SP050006Y00 (S X'FORM_ NS692417 LAN)
TL1
NS692417
RJ45 LOM circuit
+3.3V_LAN:20mils
JLOM1
SANTA_130456-511
CONN@
UL2
TC7SH08FU_SSOP5-D
GND
CHASSIS
use 40mil trace if necessary
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Compal Electronics, Inc.
LAN
LA-A891P
Monday, August 04, 2014
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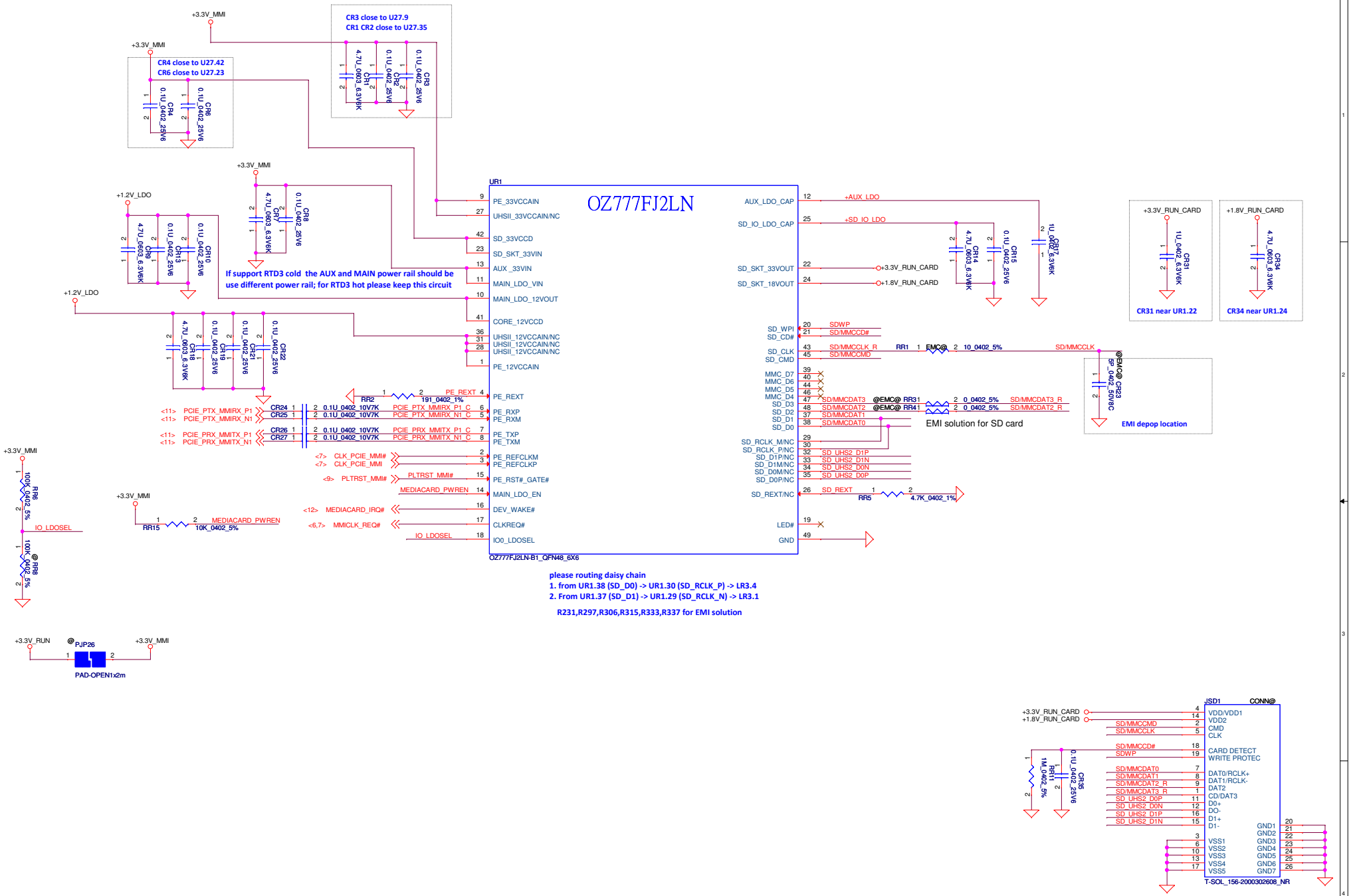

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Compal Electronics, Inc.

Title: Card Reader

Size | Document Number: LA-A891P | Rev: 1.0

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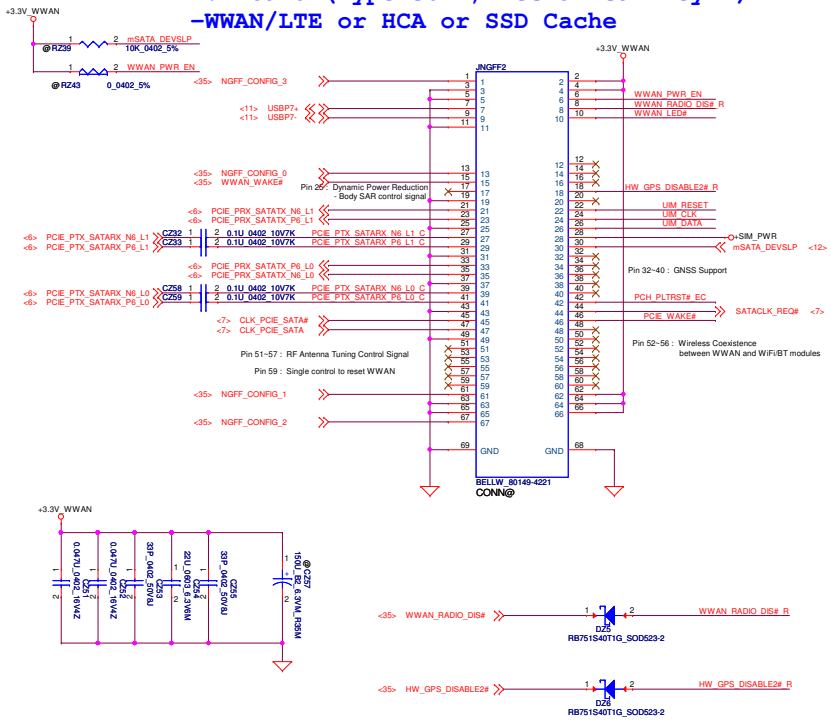
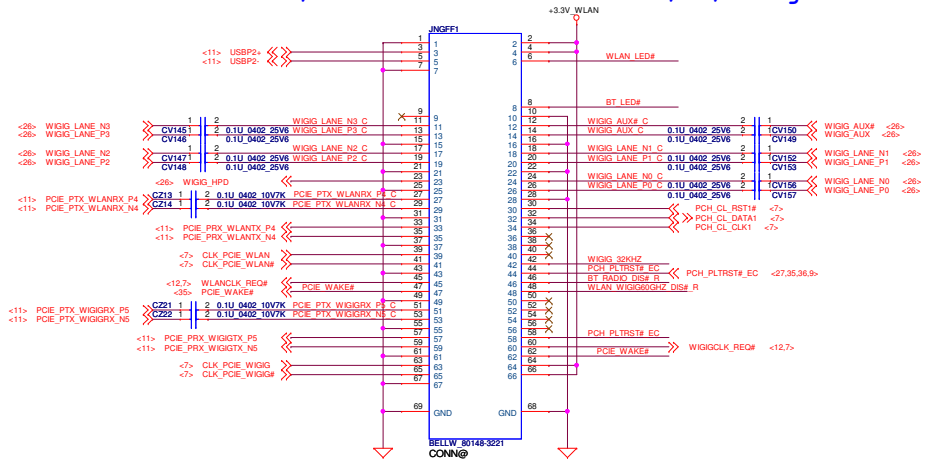
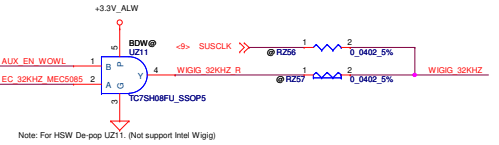
M.2 Card (Type 3042, Mechanical Key B) -WWAN/LTE or HCA or SSD Cache



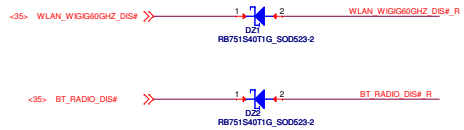
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
~~0~~	~~GND~~	~~GND~~	~~GND~~	~~GND~~	~~SSD-SATA~~
~~1~~	~~GND~~	~~HIGH~~	~~GND~~	~~GND~~	~~SSD-PCIE~~
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

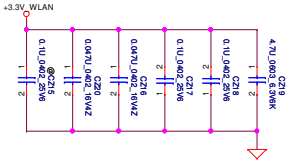
M.2 (Card. Type 3030, Mechanical Key A) -WLAN/BT Combo or TriBand WLAN/BT/WiGig



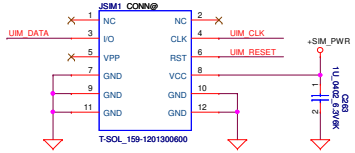


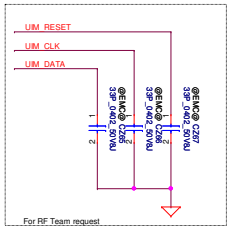
Note: For HSW De-pop UZ11. (Not support Intel Wigig)

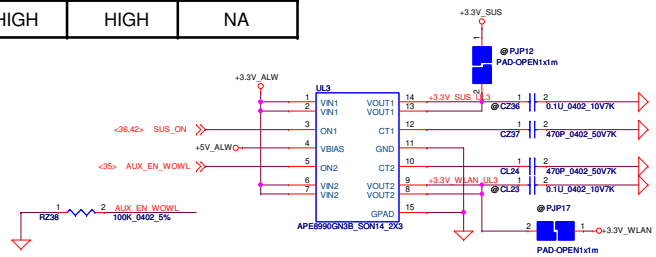


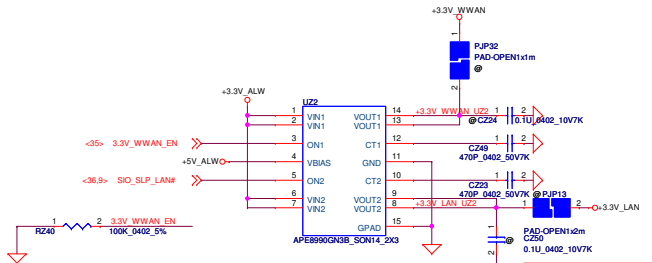


SIM Card

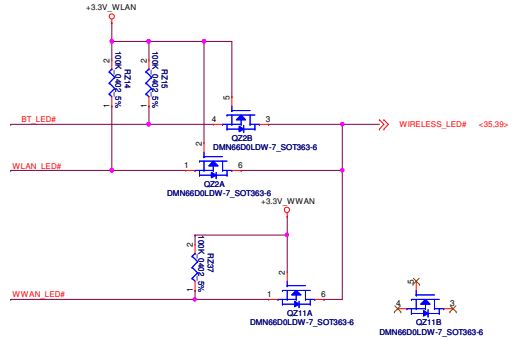








LED control circuit



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Title	NGFF Card	
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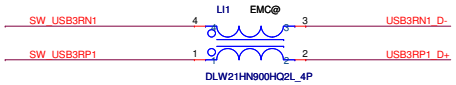
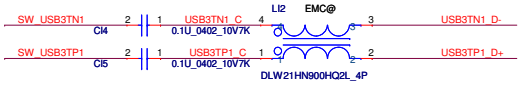
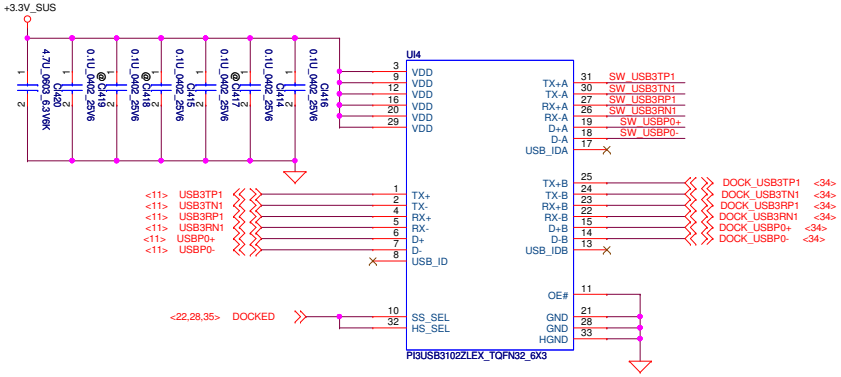
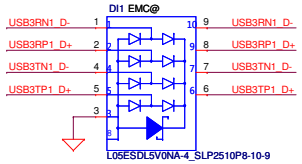


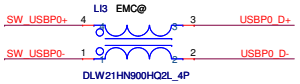




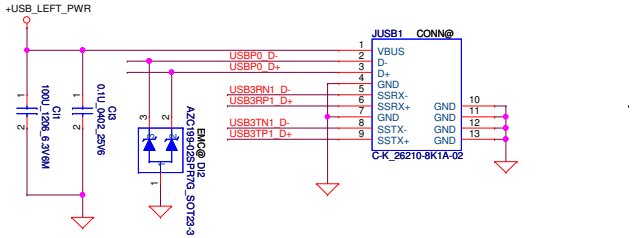
check port mapping

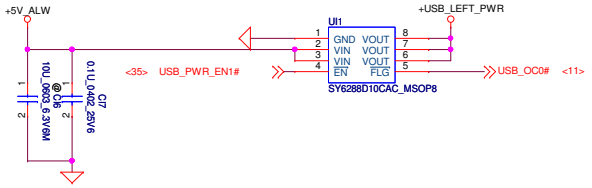
DOCKED	function
1	Dock
0	M/B

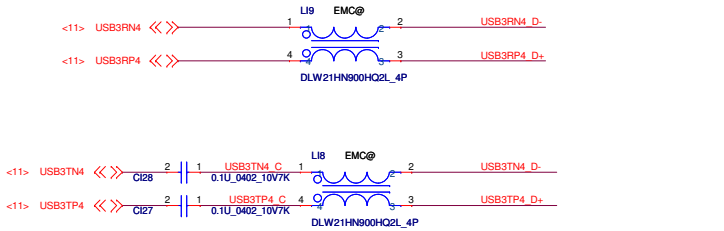


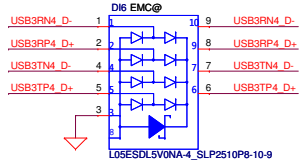


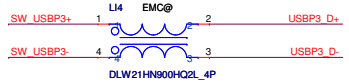
PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA

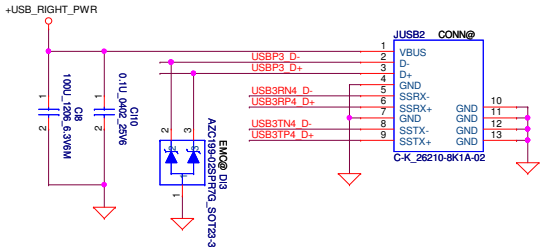


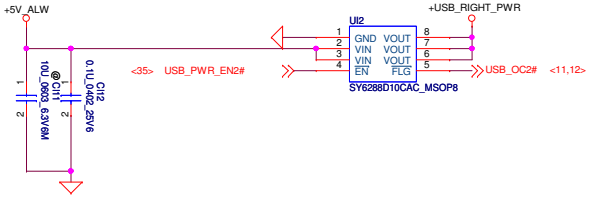


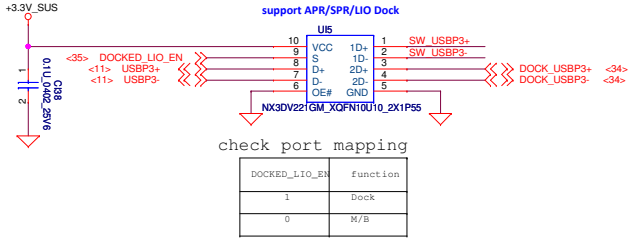












check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B

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Title: USB3.0

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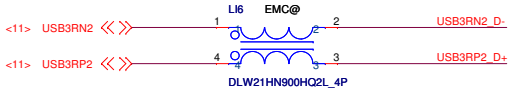

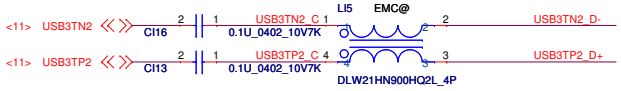

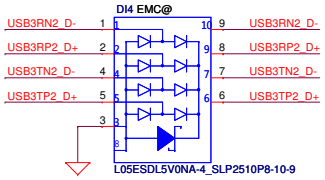

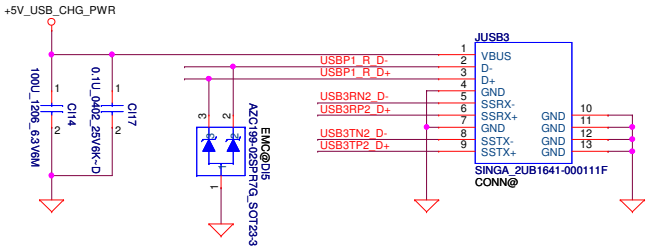

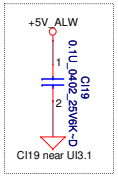

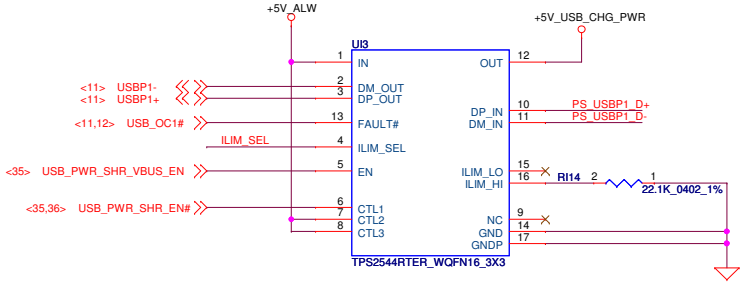

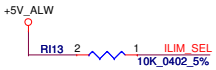

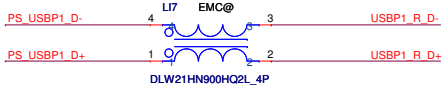

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NFC on USH/B

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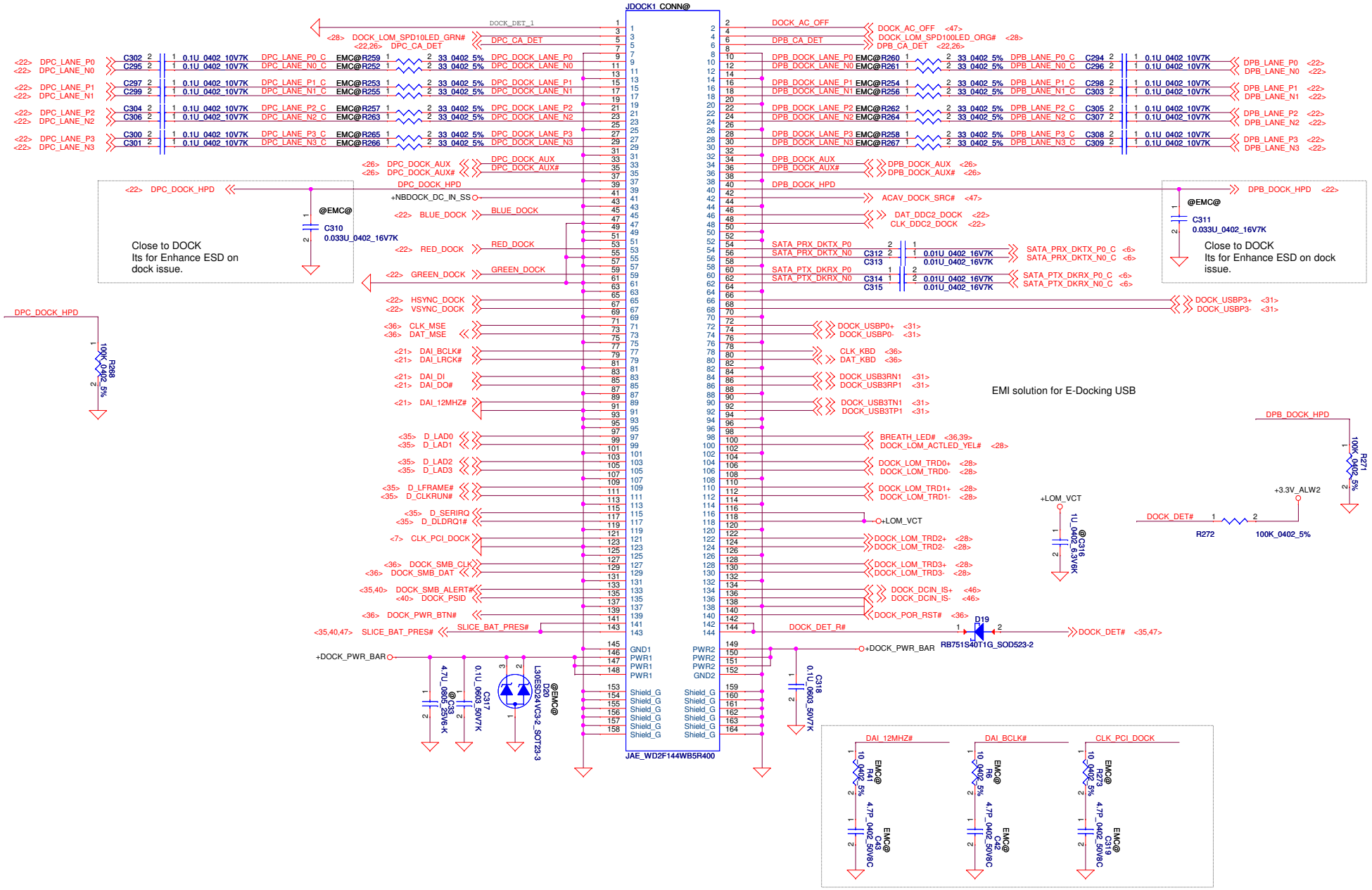
Compal Electronics, Inc.

Title: NFC

Size | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 33 of 56



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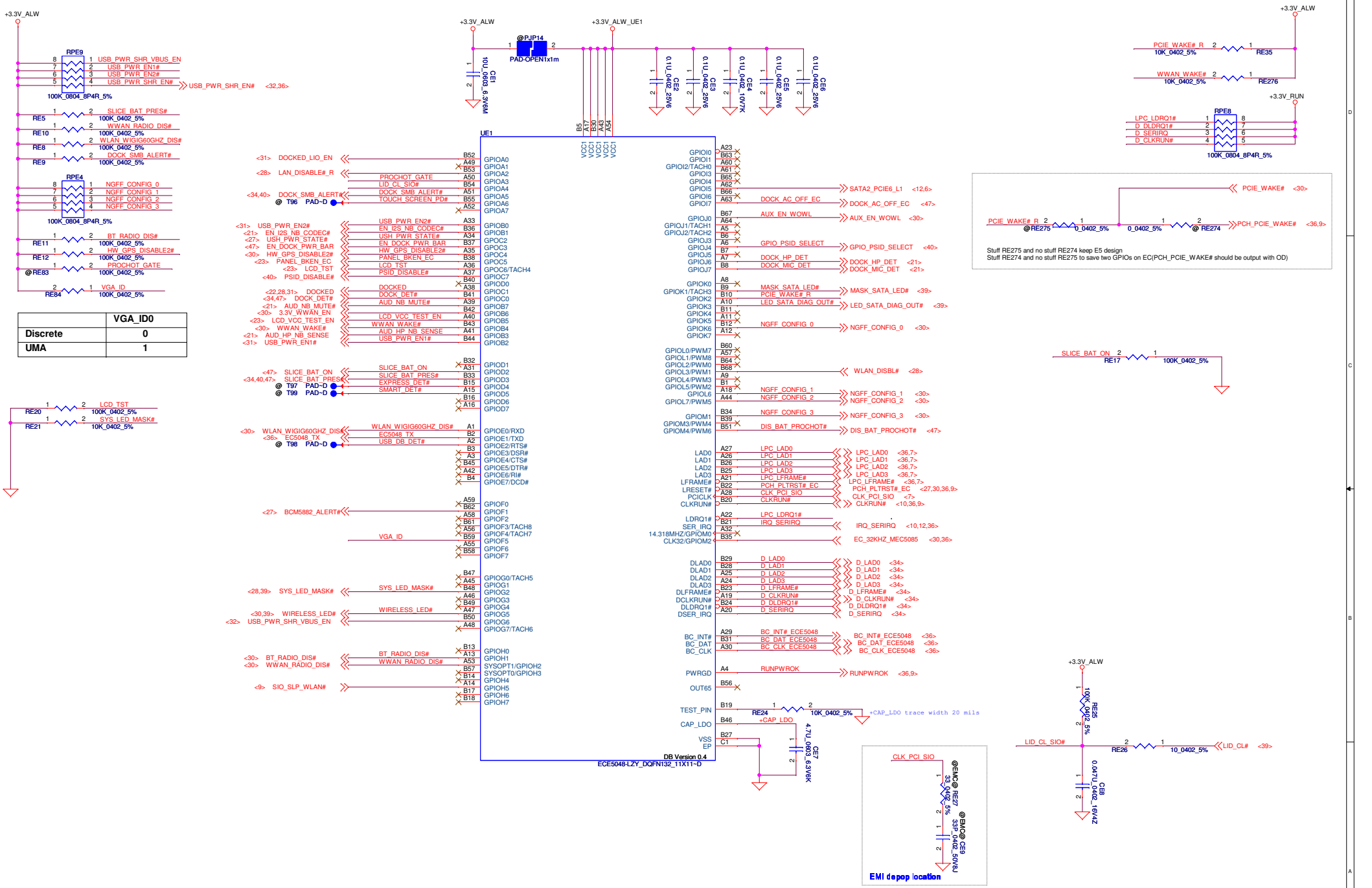
Compal Electronics, Inc.

Title: E-Dock

Size: | Document Number: LA-A891P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 34 of 56



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Title: ECE5048

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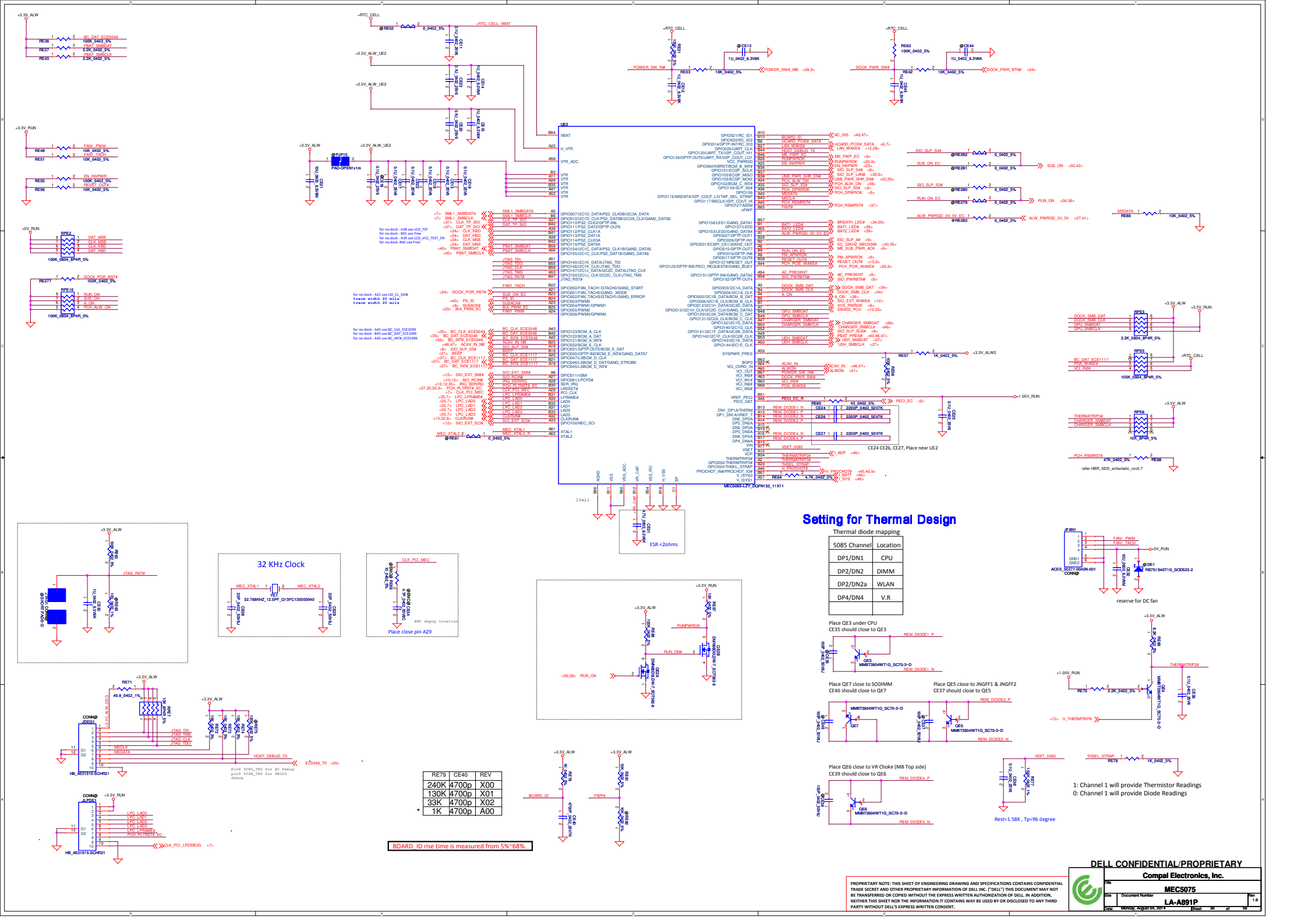
Date: Monday, August 04, 2014 | Sheet 35 of 56


Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | DIMM
DP2/DN2a | WLAN
DP4/DN4 | V.R
Place QE3 under CPU
CE35 should close to QE3
Place QE7 close to SODIMM
CE46 should close to QE7
Place QE5 close to JNGFF1 & JNGFF2
CE37 should close to QE5
Place QE6 close to VR Choke (MB Top side)
CE39 should close to QE6
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings
32 KHz Clock
32.768KHZ_12.5PF_Q13FC1350000040
ESR <2ohms
reserve for DC fan
Rest=1.58K , Tp=96 degree
RE79 | CE40 | REV
240K | 4700p | X00
130K | 4700p | X01
33K | 4700p | X02
1K | 4700p | A00
BOARD_ID rise time is measured from 5%~68%.
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MEC5075
LA-A891P
Rev 1.0
Monday, August 04, 2014
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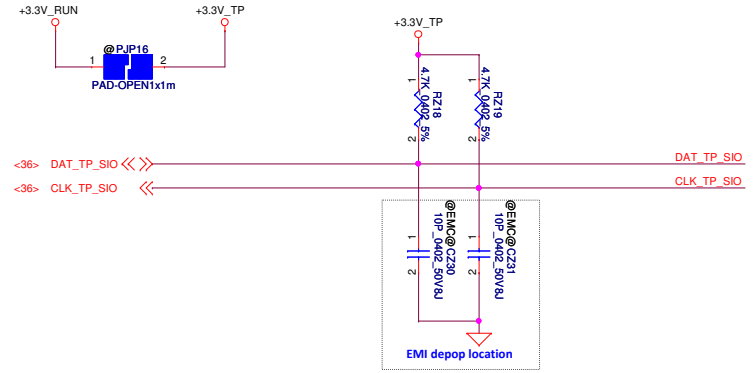
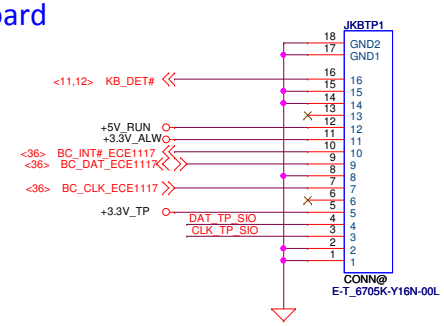
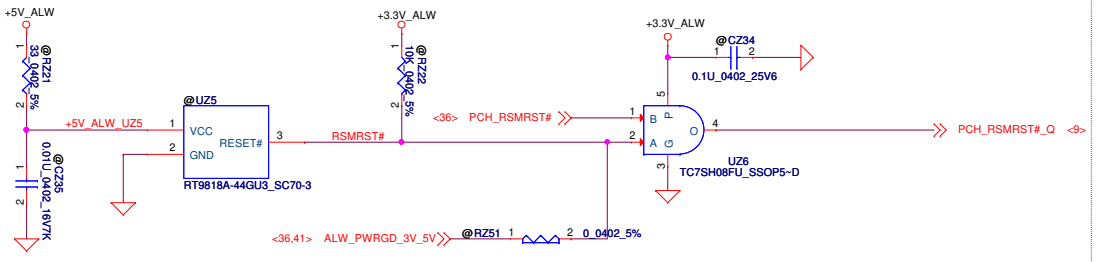
Touch Pad



Keyboard



RSMRST circuit



@IO FFC

Part Number	Description
DA30000GZ00	FPC 0VN LF-9591P REV0 M/B-IO/B

@eDP TS Cable

Part Number	Description
DC02C004S00	H-CONN SET 0VN MB-LCD-LED-CAM-TS

@eDP Cable

Part Number	Description
DC02C004T00	H-CONN SET 0VN MB-LCD-LED-CAM

@SATA Cable

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@MEDIA Board FFC

Part Number	Description
NBX0001CW00	FFC 8P G P0.5 PAD0.3 50MM MB-MEDIA/B 0VN

@KBTP FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@NFC Board FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@USH Board FFC

Part Number	Description
NBX0001CY00	FFC 20P G P0.5 PAD=0.3 75MM MB-USH/B 0VN

@FP FFC

Part Number	Description
NBX0001D100	FFC 6P G P0.5 PAD=0.3 75MM USH/B-FP 0VN

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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Compal Electronics, Inc.

Title: Keyboard

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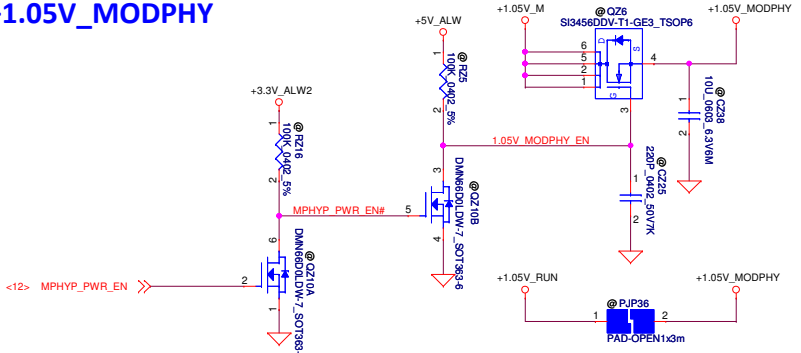
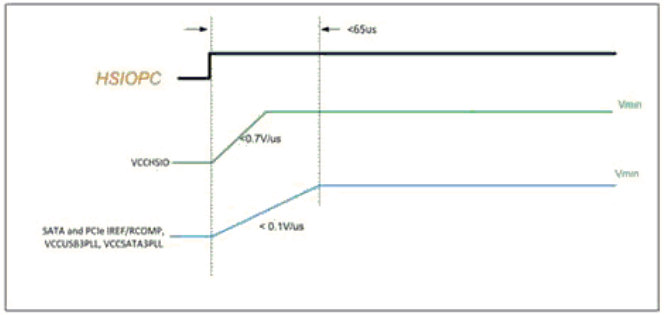
+1.05V_MODPHY



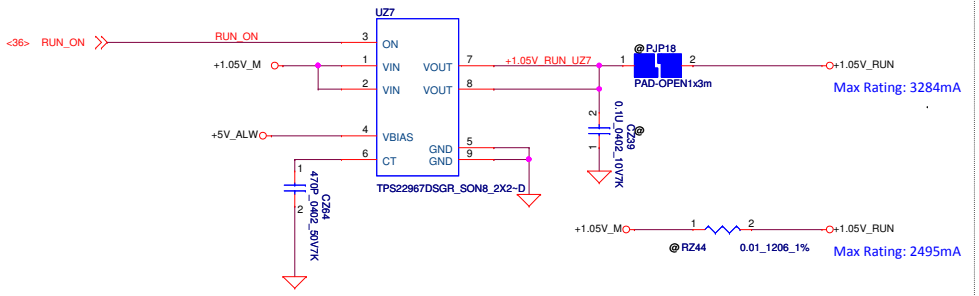
if support MODPHY off keep DSC solution

MODPHY timing spec 0.7V/us and <65us

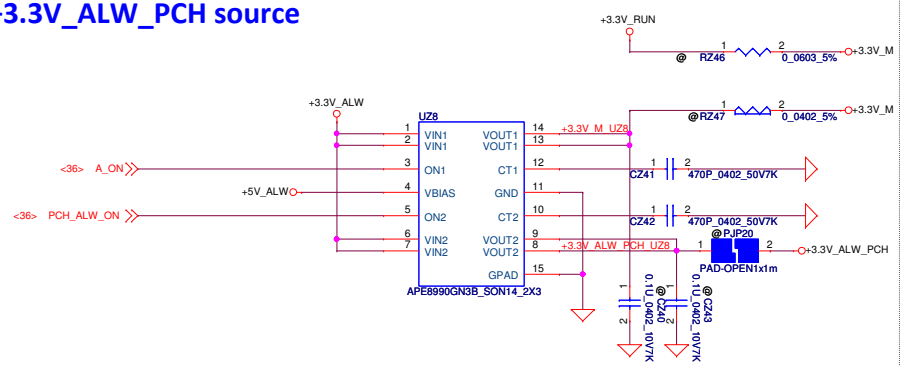
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



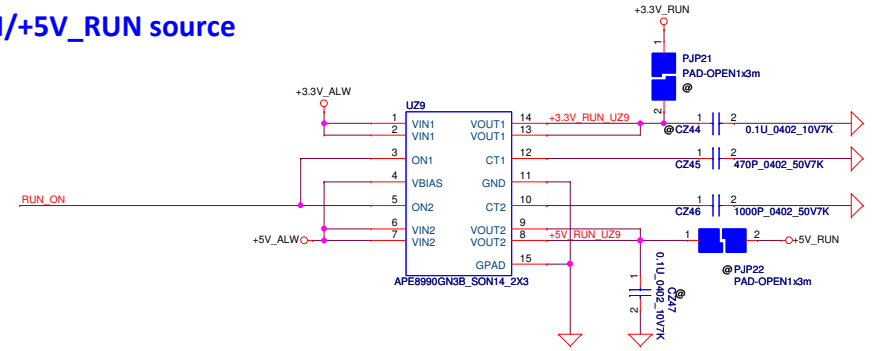
+1.05V_RUN source



+3.3V_M/+3.3V_ALW_PCH source



+3.3V_RUN/+5V_RUN source



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Compal Electronics, Inc.

Title: Power control

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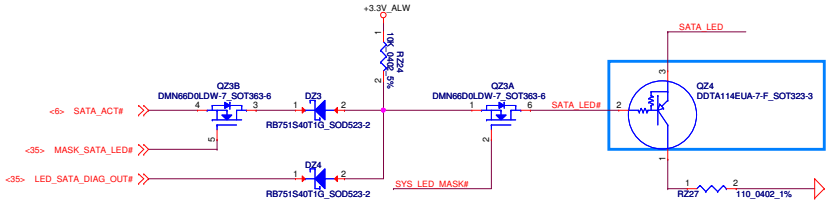
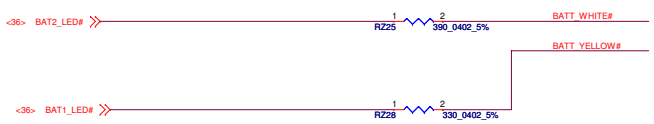
HDD LED solution for White LED



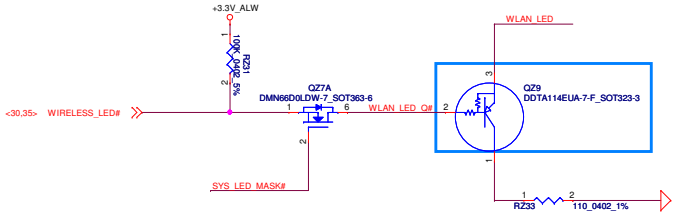
SB000002T00, S TR DDTA114EUA-7-F PNP SOT-323
(sourcer advice, but X code on ISPD)

SB000005F00 , S TR PDTA114EU PNP SC70-3
(SSI usage)

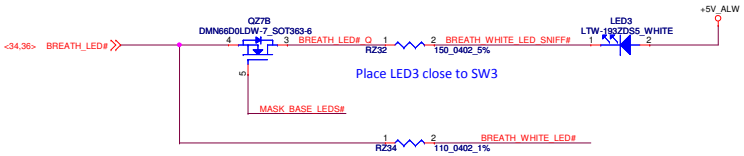
Battery LED

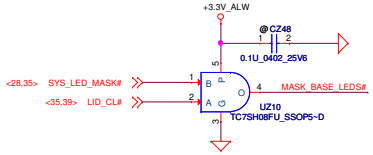


WLAN LED solution for White LED

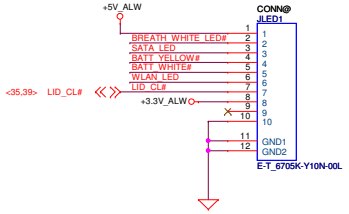


Breath LED

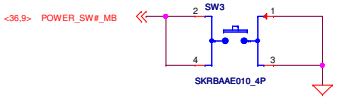




LED board CONN



POWER & INSTANT ON SWITCH



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

@H1 H_2P3, @H2 H_2P3, @H3 H_2P3, @H4 H_2P3, @H6 H_2P3, @H7 H_2P3, @H9 H_2P3, @H10 H_2P3, @H11 H_2P3, @H13 H_2P3, @H21 H_2P3, @H12 H_3P6, @H23 H_2P6N
@H19 H_3P2, @H20 H_3P2, @H22 H_3P3, @H14 H_3P5, @H15 H_3P5, @H16 H_3P5, @H17 H_3P5, @H5 H_5P6N, @H18 H_5P2X2P6N

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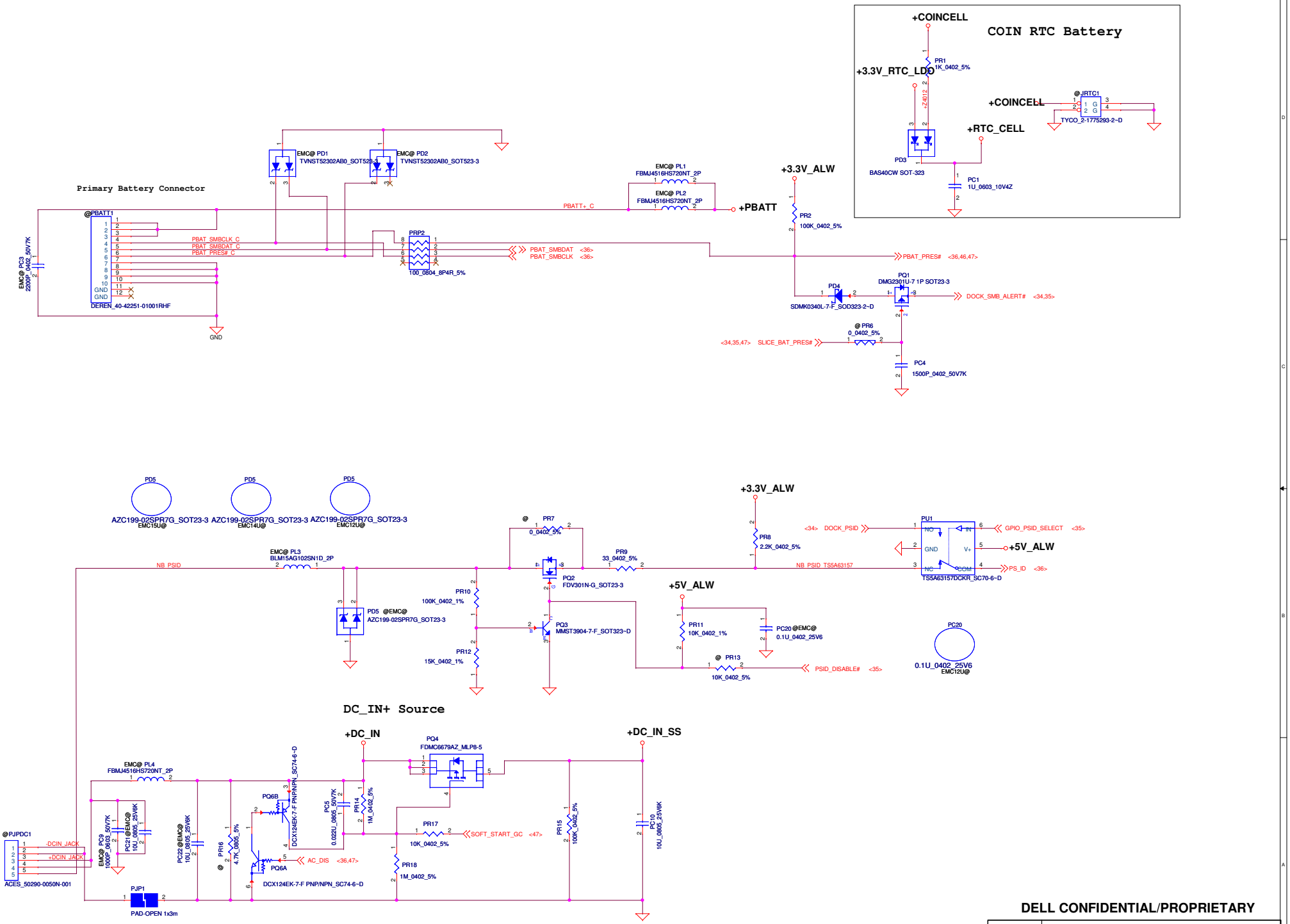
Title: PAD, LED
Size: Document Number: LA-A891P
Rev: 1.0
Date: Monday, August 04, 2014 Sheet 39 of 56



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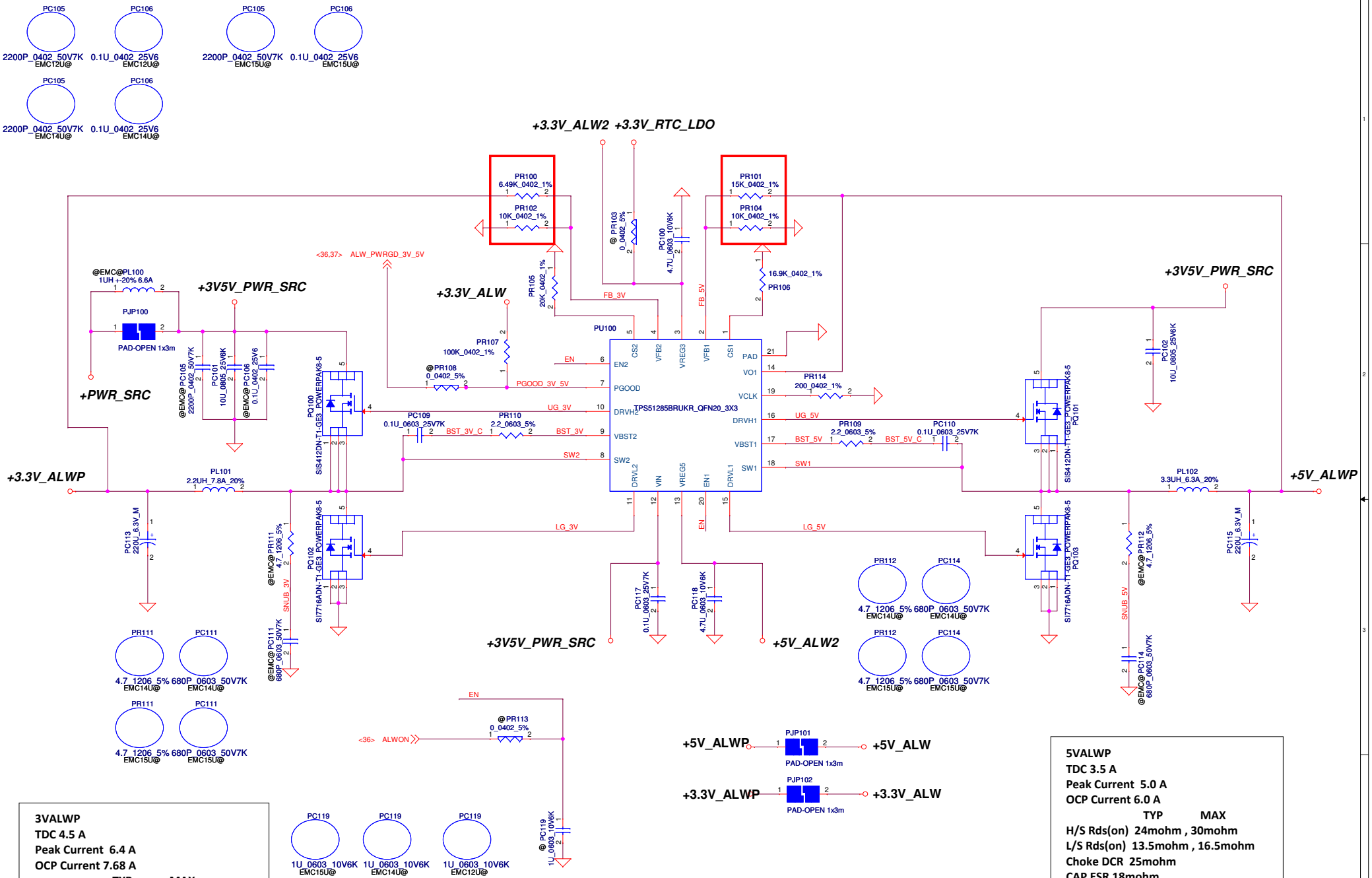
Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-A901P	Rev: 1.0
Date: Monday, August 04, 2014	Sheet 40 of 56	



3VALWP
TDC 4.5 A
Peak Current 6.4 A
OCP Current 7.68 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	15.5mohm	
CAP ESR	18mohm	

5VALWP
TDC 3.5 A
Peak Current 5.0 A
OCP Current 6.0 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	25mohm	
CAP ESR	18mohm	

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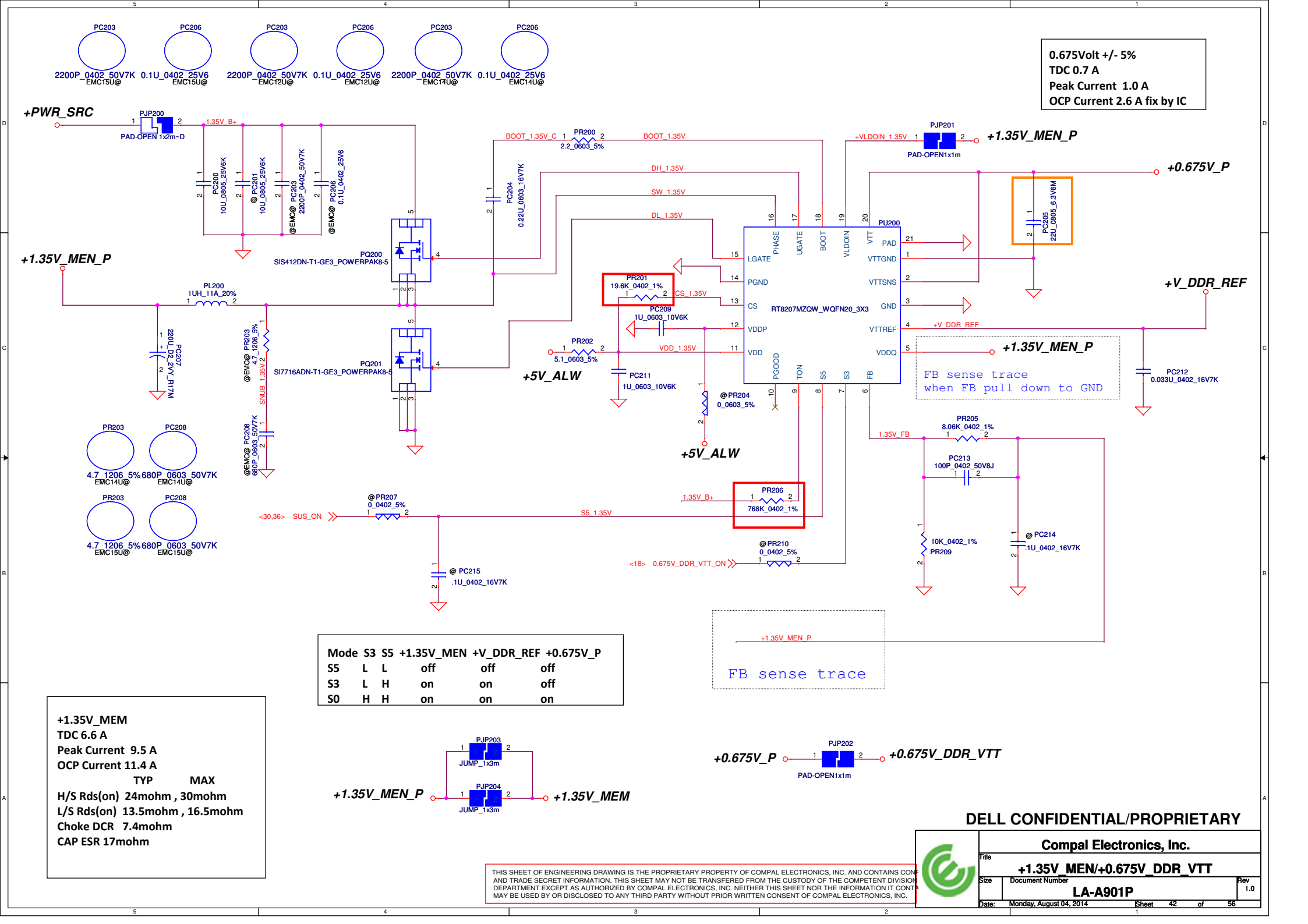
Title: +5V_ALW/3.3V_ALW

Size: | Document Number: LA-A901P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 41 of 56


0.675Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC
+PWR_SRC
PJP200
PAD-OPEN 1x2m~D
1.35V_B+
PC200 10U_0805_25V6K
@ PC201 10U_0805_25V6K
@EMC@ PC203 2200P_0402_50V7K
@EMC@ PC206 0.1U_0402_25V6
PC203 2200P_0402_50V7K EMC15U@
PC206 0.1U_0402_25V6 EMC15U@
PC203 2200P_0402_50V7K EMC12U@
PC206 0.1U_0402_25V6 EMC12U@
PC203 2200P_0402_50V7K EMC14U@
PC206 0.1U_0402_25V6 EMC14U@
+1.35V_MEN_P
PL200 1UH_11A_20%
PC207 220U_D2_2VY_R17M
@EMC@ PR203 4.7_1206_5%
SNUB_1.35V
@EMC@ PC208 680P_0603_50V7K
PR203 4.7_1206_5% EMC14U@
PC208 680P_0603_50V7K EMC14U@
PR203 4.7_1206_5% EMC15U@
PC208 680P_0603_50V7K EMC15U@
PQ200 SIS412DN-T1-GE3_POWERPAK8-5
PQ201 SI7716ADN-T1-GE3_POWERPAK8-5
BOOT_1.35V_C
PR200 2.2_0603_5%
BOOT_1.35V
PC204 0.22U_0603_16V7K
DH_1.35V
SW_1.35V
DL_1.35V
PR201 19.6K_0402_1%
CS_1.35V
PC209 1U_0603_10V6K
PR202 5.1_0603_5%
VDD_1.35V
PC211 1U_0603_10V6K
@PR204 0_0603_5%
+5V_ALW
PU200
RT8207MZQW_WQFN20_3X3
PHASE UGATE BOOT VLDOIN VTT PAD
LGATE PGND CS VDDP VDD PGOOD TON S5 S3 FB
VTTGND VTTSNS GND VTTREF VDDQ
+VLDOIN_1.35V
PJP201
PAD-OPEN1x1m
+1.35V_MEN_P
+0.675V_P
PC205 22U_0805_6.3V6M
+V_DDR_REF
+V_DDR_REF
+1.35V_MEN_P
FB sense trace
when FB pull down to GND
PC212 0.033U_0402_16V7K
PR205 8.06K_0402_1%
1.35V_FB
PC213 100P_0402_50V8J
10K_0402_1% PR209
@ PC214 .1U_0402_16V7K
@PR207 0_0402_5%
<30,36> SUS_ON
S5_1.35V
1.35V_B+
PR206 768K_0402_1%
@PR210 0_0402_5%
<18> 0.675V_DDR_VTT_ON
@ PC215 .1U_0402_16V7K
+1.35V_MEN_P
FB sense trace
Mode S3 S5 +1.35V_MEN +V_DDR_REF +0.675V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
+1.35V_MEM
TDC 6.6 A
Peak Current 9.5 A
OCP Current 11.4 A
TYP MAX
H/S Rds(on) 24mohm , 30mohm
L/S Rds(on) 13.5mohm , 16.5mohm
Choke DCR 7.4mohm
CAP ESR 17mohm
PJP203
JUMP_1x3m
PJP204
JUMP_1x3m
+1.35V_MEN_P
+1.35V_MEM
+0.675V_P
PJP202
PAD-OPEN1x1m
+0.675V_DDR_VTT
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Compal Electronics, Inc.
Title
+1.35V_MEN/+0.675V_DDR_VTT
Size
Document Number
LA-A901P
Rev
1.0
Date: Monday, August 04, 2014
Sheet 42 of 56
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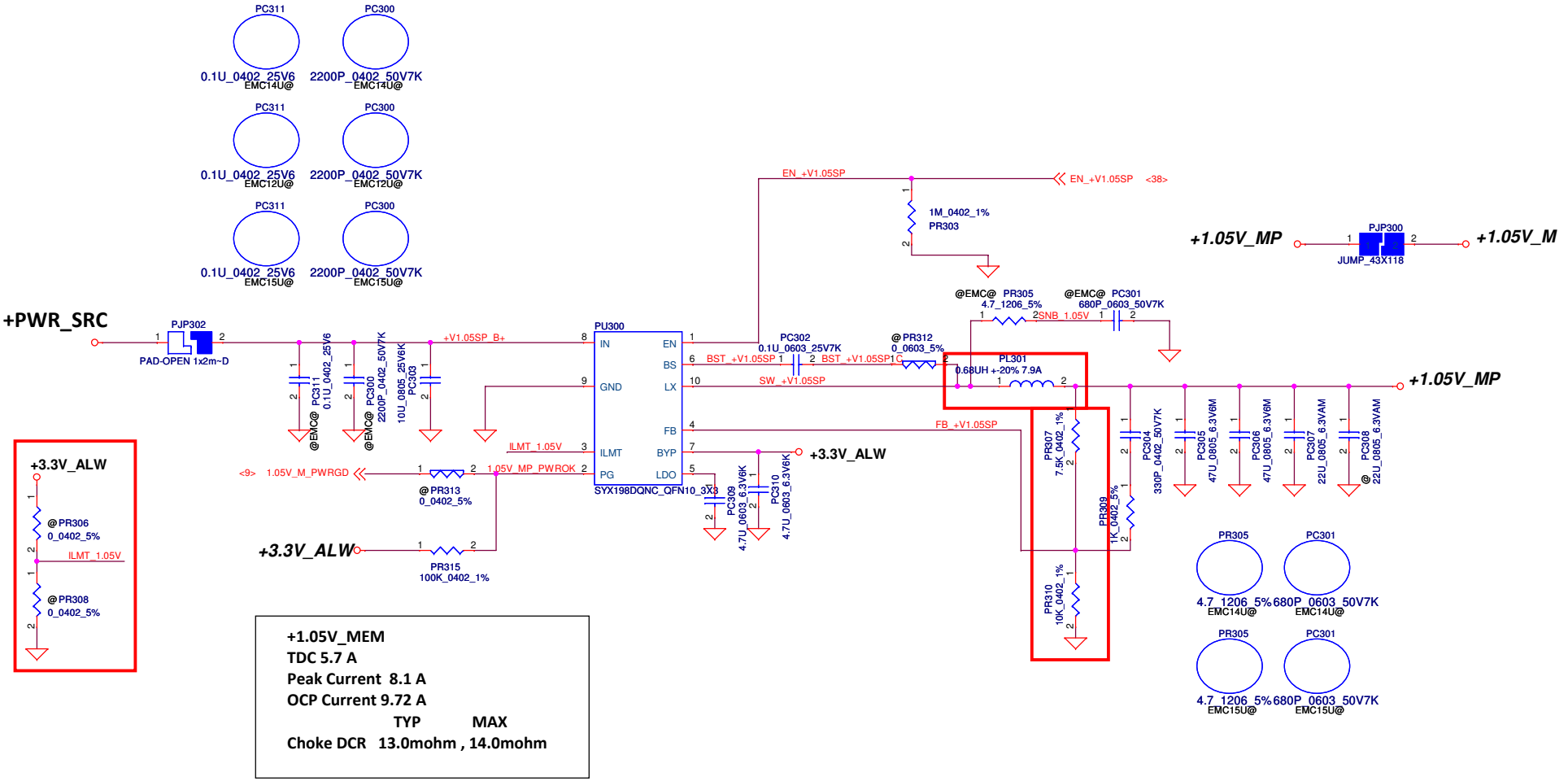

+1.05V_MEM
TDC 5.7 A
Peak Current 8.1 A
OCP Current 9.72 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

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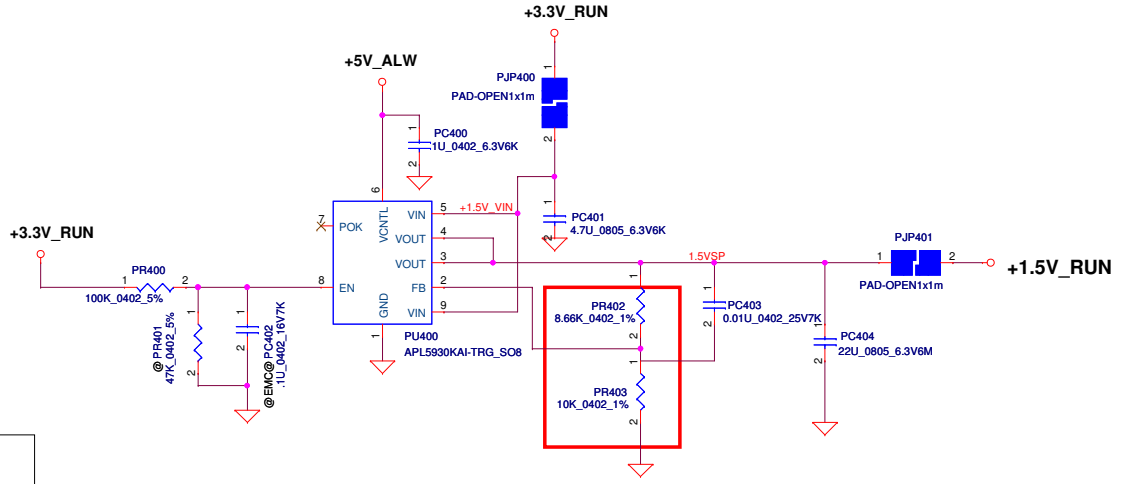
Compal Electronics, Inc.		
Title: +1.05V_M		
Size	Document Number: LA-A901P	Rev: 1.0
Date: Monday, August 04, 2014	Sheet 43 of 56	



+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

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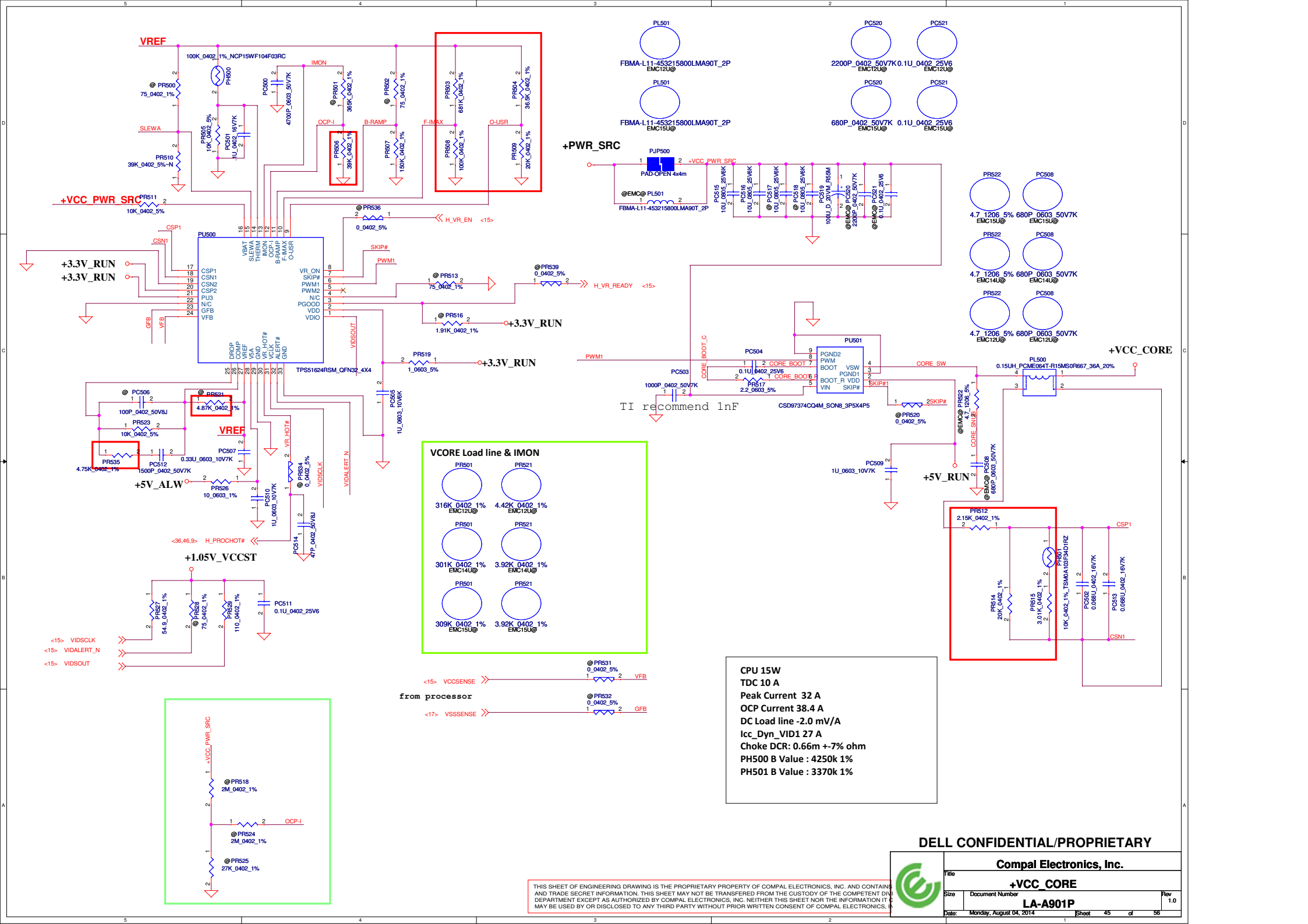
Compal Electronics, Inc.		
Title: +1.5V_RUN		
Size	Document Number: LA-A901P	Rev: 1.0
Date: Monday, August 04, 2014	Sheet 44 of 56	


VREF
100K_0402_1%_NCP15WF104F03RC
PH500
IMON
OCP-I
B-RAMP
F-IMAX
O-USR
SLEWA
+VCC_PWR_SRC
PU500
TPS51624RSM_QFN32_4X4
+3.3V_RUN
+3.3V_RUN
H_VR_EN <15>
H_VR_READY <15>
SKIP#
PWM1
VIDSOUT
VIDSCLK
VIDALERT_N
VR_HOT#
+5V_ALW
+1.05V_VCCST
<36,46,9> H_PROCHOT#
<15> VIDSCLK
<15> VIDALERT_N
<15> VIDSOUT
VCORE Load line & IMON
316K_0402_1% EMC12U@
4.42K_0402_1% EMC12U@
301K_0402_1% EMC14U@
3.92K_0402_1% EMC14U@
309K_0402_1% EMC15U@
3.92K_0402_1% EMC15U@
<15> VCCSENSE
<17> VSSSENSE
from processor
VFB
GFB
+VCC_PWR_SRC
@PR518 2M_0402_1%
OCP-I
@PR524 2M_0402_1%
@PR525 27K_0402_1%
FBMA-L11-453215800LMA90T_2P EMC12U@
FBMA-L11-453215800LMA90T_2P EMC15U@
2200P_0402_50V7K 0.1U_0402_25V6 EMC12U@
680P_0402_50V7K 0.1U_0402_25V6 EMC15U@
+PWR_SRC
PJP500
PAD-OPEN 4x4m
+VCC_PWR_SRC
FBMA-L11-453215800LMA90T_2P
4.7_1206_5% 680P_0603_50V7K EMC15U@
4.7_1206_5% 680P_0603_50V7K EMC14U@
4.7_1206_5% 680P_0603_50V7K EMC12U@
PU501
CSD97374CQ4M_SON8_3P5X4P5
TI recommend 1nF
+VCC_CORE
PL500
0.15UH_PCME064T-R15MS0R667_36A_20%
+5V_RUN
CSP1
CSN1
PH501
10K_0402_1%_TSM0A103F34D1RZ
CPU 15W
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
DC Load line -2.0 mV/A
Icc_Dyn_VID1 27 A
Choke DCR: 0.66m +-7% ohm
PH500 B Value : 4250k 1%
PH501 B Value : 3370k 1%
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Compal Electronics, Inc.
+VCC_CORE
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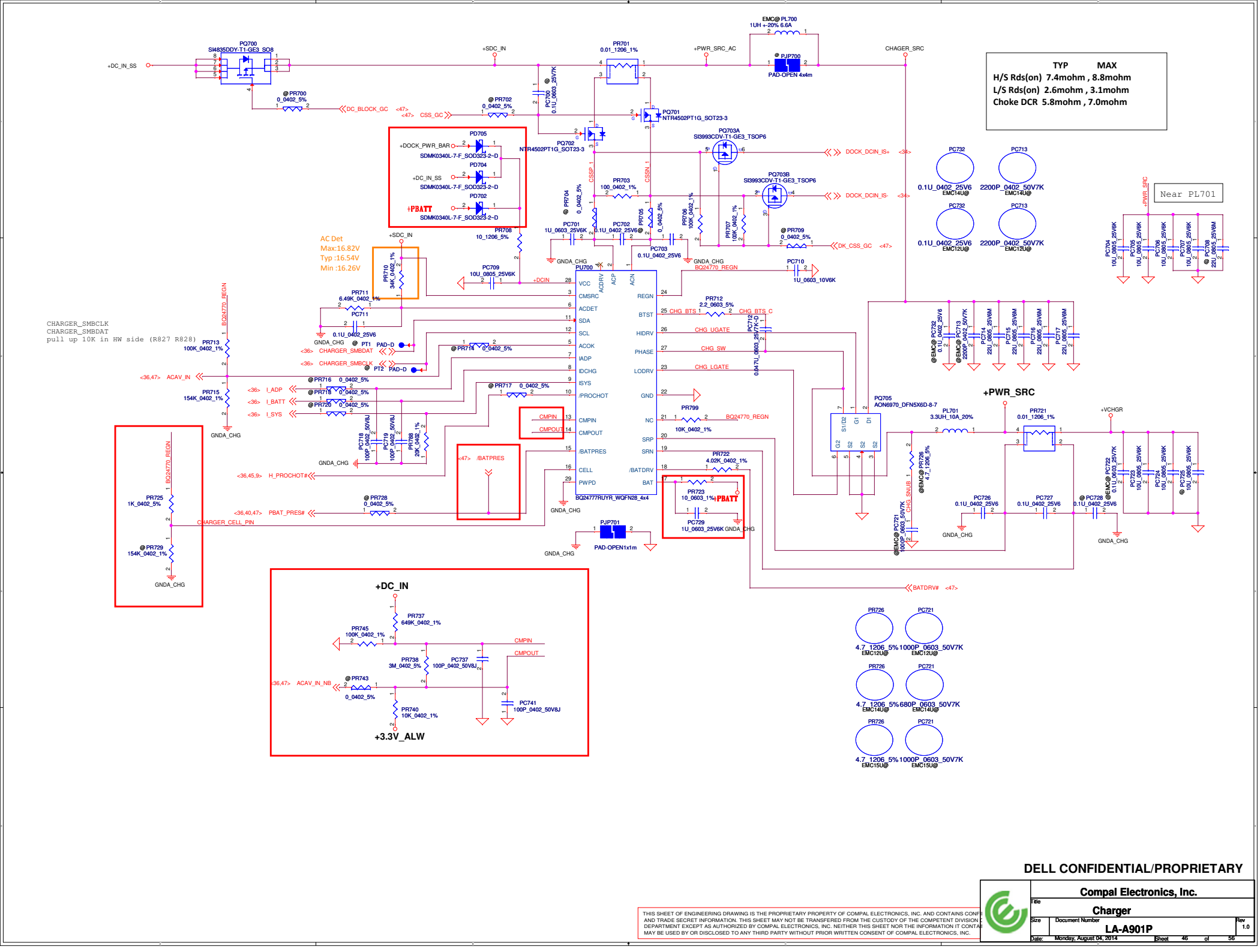

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Title: Charger	
Size:	Document Number: LA-A901P
Rev: 1.0	
Date: Monday, August 04, 2014	Sheet 46 of 56

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Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.

Vth=0.5-1.5V

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Title: Selector
Size: Document Number: LA-A901P
Rev: 1.0
Date: Monday, August 04, 2014
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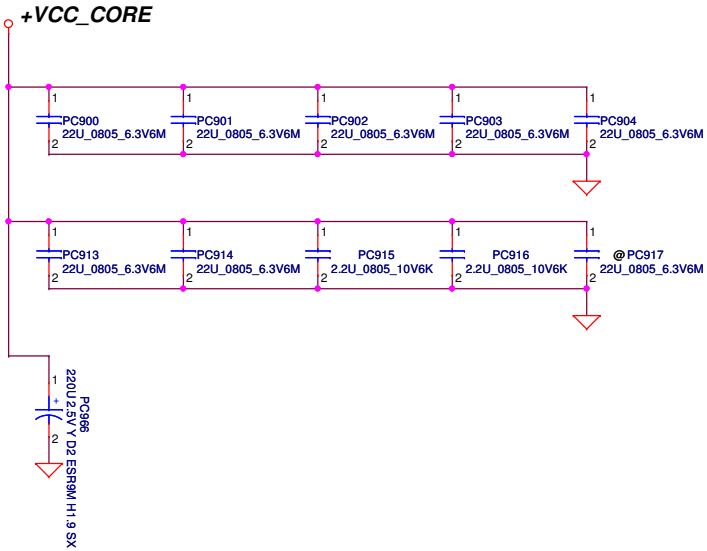

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Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size | Document Number: LA-A901P | Rev: 1.0

Date: Monday, August 04, 2014 | Sheet 48 of 56

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 (0.1uF)	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111,PC111,PR112,PC114,PR203,PC208,PR305,PC301,PR522,PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01
11	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
12	46	Charger	3/03	Compal	To set OVP level	depop PR729 change PR725 to 1k	X02
13	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
14	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
15	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02
16	40	DCIN	3/03	Compal	For ME change request	Change PJPDC1	X02
17	46	Charger	3/20	Compal	To avoid unplug AC shutdown, there is no AC off signal in BIOS set up menu	Change PR710 to 34k Change PR711 to 6.49k	X02

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
18	46	Charger	5/22	TI	To prevent acoustic noise issue	PL701 change from 2.2uH to 3.3uH	X03
19	40	DCIN	5/22	Compal	For ME change request	Change PBATT1	X03

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2		HW	2013/10/8	COMPAL			0.2(X01)
3	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
4	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01) 0.2(X01)
5	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. add QV20,CZ69,RV210,RV212,QV21 external FET switch circuit 7. UV8 pin B5, B6 change to +3.3V_RUN_VMM 8. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 9. Depop RV73 10. add LP_EN on UV8.A5 (10/18) 11. depop QV20,CZ69,RV210,RV212, QV21 external FET switch circuit (10/24) 12.RPV2 pin1 & pin2 NC (11/4)	0.2(X01)
6	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2(X01)
7	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2(X01)
8	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, , reserved RC27.	0.2(X01)
9	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
10	24	HW	2013/10/9	COMPAL	Correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2(X01)
11	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)

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12	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
13	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2(X01)
14	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
15	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	remove QZ5, QZ7.2 & QZ3.2 change to SYS_LED_MASK#	0.2(X01)
16	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	add UN3, CN3, CN4, PJP7 and reserved it.	0.2(X01)
17	30,36	HW	2013/10/17	COMPAL	follow Dell requirement.	add back SUS_ON, change +3.3V_SUS control pin to SIO_SLP_S4# 1. UL3.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282(Pop), RE281(depop) 4. add RE279, RE280 (dock only) 5. UE2.B9 → RUN_ON_EC	0.2(X01)
18	40	HW	2013/10/18	COMPAL	crystal EA finetune.	add RV520 on YV1.3	0.2(X01)
19	23	HW	2013/10/18	COMPAL	follow ESD recommend.	LZ1 change from SM070001N00 to SM070003Y00	0.2(X01)
20	32	HW	2013/10/24	COMPAL	Base on EA result.	remove UI6 USB3 repeater and srounding componet.	0.2(X01)
21	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4 to replace PCH_GPIO48, remove	0.2(X01)
22	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2(X01)
23	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
24	30	HW	2013/10/29	COMPAL	New SIM connector has no this pin.	remove UIM_DET on JNGFF2 pin58	0.2(X01)
25	23	HW	2013/10/29	COMPAL	it's designed for Goliad, Houston doesn't need.	remove RZ1	0.2(X01)
26	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ43, 100k pull up for WWAN_PWR_EN	0.2(X01)
27	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)

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28	37	HW	2013/10/29	COMPAL	Dell request.	add RZ48, RZ49, QZ12 depop UZ5, UZ6, RZ21, RZ22, CZ35,RC91 (11/4) add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88 (11/4)	0.2(X01)
29	44	HW	2013/10/29	COMPAL	delete double parts.	Delete RV185	0.2(X01)
30	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)
31	28	HW	2013/11/04	COMPAL	SSI design will cause LED behavior error.	Change QL1, QL2 contorl pin from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)
32	21	HW	2013/11/04	COMPAL	EMC request.	Add RA42, RA43.	0.2(X01)
33	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2(X01)
34	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2(X01)
35	40	HW	2013/11/05	COMPAL	to prevent backdrive	add DV9 for 3.3v_GFX_AON	0.2(X01)
36	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2(X01)
37	7,40	HW	2013/11/06	COMPAL	follow xtal vender? suggest	CC8,CC11 change from 18pF to 15pF CV34,CV35 change from 10pF to 15pF	0.2(X01)
38	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN9,RN11,RN13,RN16 pop 0ohm	0.2(X01)
39	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3(X01)
40	22	HW	2013/12/17	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.3(X01)
41	22	HW	2013/12/17	COMPAL	To solve CRT display jitter issue	1.LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D 2.CV90,CV101 change from 1uF to 10uF	0.3(X01)
42	22	HW	2013/12/17	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2. remove QZ12,RZ48,RZ49,RZ50	0.3(X01)
43	22	HW	2013/12/17	COMPAL	Base on EA result to modify R value	Change RL21~RL28 from 5.6K to 2.2K	0.3(X01)

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44	15	HW	2013/12/17	COMPAL	EMI request	add CC94, CC95, CC96	0.3(X01)
45	22	HW	2013/12/17	COMPAL	follow vender suggestion	"1. change LV22 , LV24 From SM01000N400 S SUPPRE_ MURATA BLM15AX102SN1D 0402 To SM01000NO00 S SUPPRE_ MURATA BLM15PX181SN1D 0402 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to +1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO"	0.3(X01)
46	28，39	HW	2013/12/17	COMPAL	Because TPS22965 is X1 code	For Dock, UN3,UZ7 change fron TPS22965 to SA000070S002. For Entry, UN3,UZ3 change fron TPS22965 to SA000070S00	0.3(X01)
47	34	HW	2013/12/18	COMPAL	To solve Power leakage issue.	For Dock, UN3,UZ7 change fron TPS22965 to SA000070S002. For Entry, UN3,UZ3 change fron TPS22965 to SA000070S00	0.3(X01)
48	26	HW	2014/02/07	COMPAL	Base on PS8338 datasheet, PI0 have 2 level, PI1 have 3 level	For PI0, delete RV621 (H12) For PI1, add RV100 PD to GND	0.4(X01)
49	38	HW	2014/02/07	COMPAL	For no support MODPHY	1.PJP36 pin1 from +1.05V_M to +1.05V_RUN 2.depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.4(X01)
50	36	HW	2014/02/07	COMPAL	EC request, for Delray common code reserved.	Add RE283	0.4(X01)
51	9, 16	HW	2014/02/07	COMPAL	Follow intel DG 1.2	Reserved 0.47uF between +PCH_VCCDSW3_3 and +PCH_VCCDSW Reserved RC92 to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE.	0.4(X01)
52	34	HW	2014/03/04	COMPAL	follow EMI request	pop R41, R6, R273 ; R273 change to 10 ohm. Pop C42, C43, C319 ; C319 change to 4.7pF	0.4(X01)
53	30	HW	2014/03/04	COMPAL	intel Wigig need 32K clock when DSx	1.Add UZ11&RZ56(@)&RZ57 2.UE2.B2 add EC_32KHZ_MEC5085 3.JNGFF1 change to WIGIG_32KHZ from SUSCLK	0.4(X01)
54	20	HW	2014/03/04	COMPAL	To add 3rd source repeater, Parade, needs more control pin	1. add RN22, RN23, RN24, RN25 2. Change RN19 from 4.7K to 4.99K	0.4(X01)
55	39	HW	2014/03/04	COMPAL	Fine to current limited resistor to	Change RZ27, RZ33, RZ34 to 110 ohm	0.4(X01)
56	6	HW	2014/05/19	COMPAL	RTC X'tal EA test pass, remove reserve component.	RC4 change to short pad.	0.5(X02)
57	38	HW	2014/05/19	COMPAL	power sequence can't meet timing.	RZ42 change to short pad.	0.5(X02)
58	38	HW	2014/05/19	COMPAL	power sequence can't meet timing.	Remove UZ7, CZ64 BOM structure VPRO@.	0.5(X02)
59	18,19	HW	2014/05/19	COMPAL	For ESD restart issue: Contact +/-4kV on screws to cause system restart.	stuff CD6 and change BOM struture to EMC@.	0.5(X02)
60	15	HW	2014/05/19	COMPAL	For ESD restart issue: Contact +/-4kV on screws to cause system restart.	stuff CC23, CC79, CC84, CC85.	0.5(X02)

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61	38	HW	2014/05/19	COMPAL	+3.3V_M test pass, remove reserve component.	RZ47 change to short pad.	0.5(X02)
62	30	HW	2014/05/19	COMPAL	WiGig function test pass, remove reserve component.	RZ57 change to short pad.	0.5(X02)
63	28	HW	2014/05/19	COMPAL	change LAN chip from tray to tape & reel.	change LAN chip from SA000066W5L to SA000066W3L	0.5(X02)
64	36	HW	2014/05/19	COMPAL	Change Board ID to X02.	RE79 change from 130K to 33K.	0.5(X02)
65	21	HW	2014/05/21	COMPAL	SMT connector shift issue.	change JHP1 to SINGA_2SJ3080-039111F.	0.5(X02)
66	12	HW	2014/05/21	COMPAL	For BDW & HSW CPU detect	1. Net name change from PCH_GPIO67 to CPU_SEL. 2. add RC163(@) & RC306.	0.5(X02)
67	36	HW	2014/07/04	COMPAL	Change Board ID to A00.	RE79 change from 33K to 1K.	1.0(A00)
~~68~~	~~36~~	~~HW~~	~~2014/07/04~~	~~COMPAL~~	~~Thermal event Issue~~	~~Co-lay H_VR_EN connect to RE70.1 and reserve RE284 to switch.~~	~~1.0(A00)~~
~~69~~	~~29~~	~~HW~~	~~2014/07/04~~	~~COMPAL~~	~~Fix BIOS post time issue.~~	~~No stuff RR11, CR35.~~	~~1.0(A00)~~
70	06	HW	2014/07/04	COMPAL	Service Mode Switch	Change RC2 & SW1 to BDW@, and RC301 to HSW@.	1.0(A00)
71	28	HW	2014/07/04	COMPAL	BITS152312_WLAN issue.	Add 1M PU on LOM_SPD100LED_ORG# and LOM_SPD10LED_GRN#.	1.0(A00)
72	39	HW	2014/07/04	COMPAL	To fix WLAN/WWAN standoff dropped issue.	H19 and H20 change from 3.3mm to 3.2mm.	1.0(A00)
~~73~~	~~22~~	~~HW~~	~~2014/07/11~~	~~COMPAL~~	~~To fix power supply sequence issue.~~	~~UV8 change from SA00007G810 to SA00007G820.~~	~~1.0(A00)~~
74	36	HW	2014/07/14	COMPAL	In order to meet crystal EA.	CE28 and CE29 change from 27P to 33P.	1.0(A00)
75	28, 35	HW	2014/07/15	COMPAL	BITS152312_WLAN issue.	change net name from WLAN_LAN_DISBL# to WLAN_DISBL#	1.0(A00)

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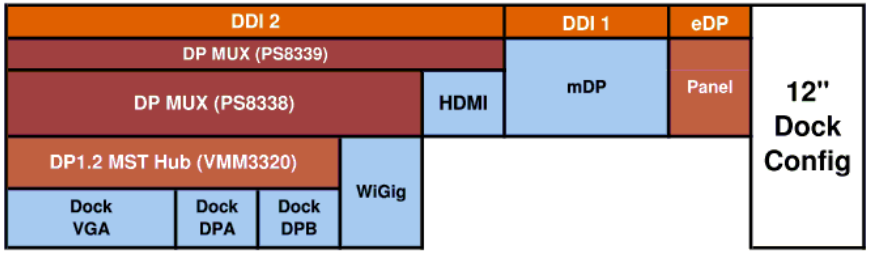

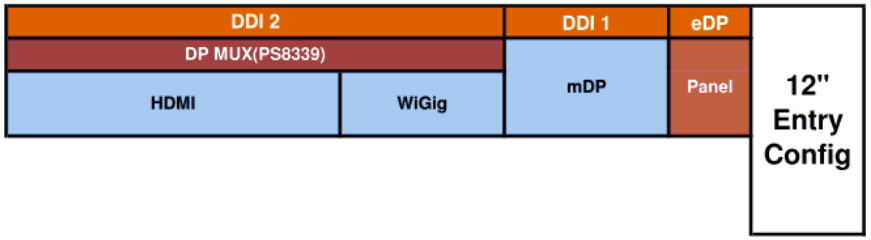

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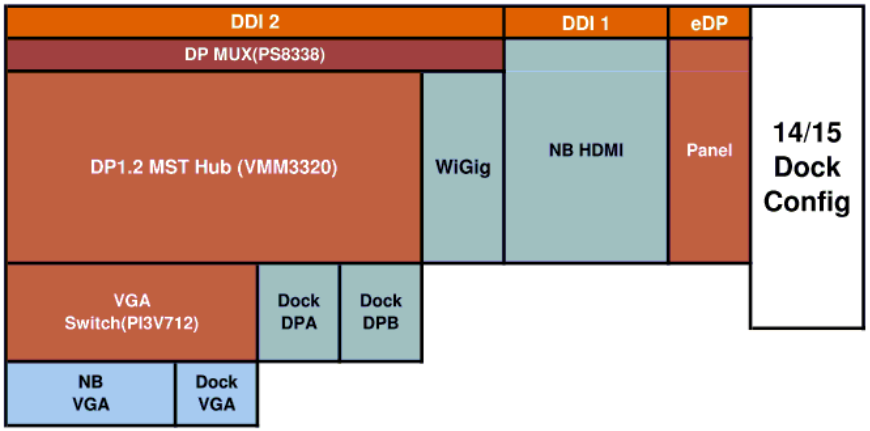

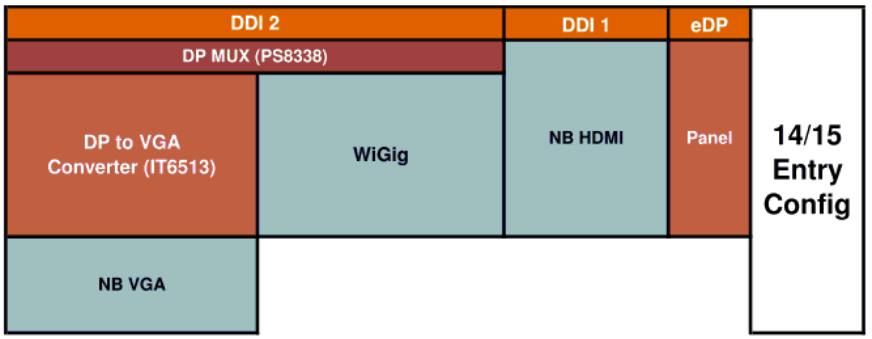

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